10 kHz - 1024 MHz
AM/FM SIGNAL GENERATOR
2017

Code No. 52017-900K

Serial Nos. commencing 118202

AMENDMENT RECORD

The following amendments are incorporated in this manual.

Amendment No.	*Date*	*Applies to Ser. Nos. commencing*

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MARCONI INSTRUMENTS LIMITED
ST. ALBANS HERTFORDSHIRE ENGLAND.

Part No. 46881-389T

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} These chapters are contained in a separate Operating Manual Vol. 1

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HAZARD WARNING SYMBOLS

The following symbols appear on the equipment.

Symbol	*Type of hazard*	*Reference in manual*
⚠	Static sensitive device	Page (iv)
⚠	Incorrect adjustment	Chap. 3, para. 30
⚠ BERYLLIA	Component containing beryllia	Page (iv)
⚠	AC voltages	Chap. 4-2, para. 265

Note...

Each page bears the date of the original issue or the code number and date of the latest amendment (Am. 1, Am. 2 etc.). New or amended material of technical importance introduced by the latest amendment is indicated by triangles positioned thus ▶.....◀ to show the extent of the change. When a chapter is reissued the triangles do not appear. Any changes subsequent to the latest amendment state of the manual are included on inserted sheets coded C1, C2 etc.

NOTES AND CAUTIONS

ELECTRICAL SAFETY PRECAUTIONS

This equipment is protected in accordance with IEC Safety Class 1. It has been designed and tested according to IEC Publication 348, 'Safety Requirements for Electronic Measuring Apparatus', and has been supplied in a safe condition. The following precautions must be observed by the user to ensure safe operation and to retain the equipment in a safe condition.

Defects and abnormal stresses

Whenever it is likely that protection has been impaired, for example as a result of damage caused by severe conditions of transport or storage, the equipment shall be made inoperative and be secured against any unintended operation.

Removal of covers

Removal of the covers is likely to expose live parts although reasonable precautions have been taken in the design of the equipment to shield such parts. The equipment shall be disconnected from the supply before carrying out any adjustment, replacement or maintenance and repair during which the equipment shall be opened. If any adjustment, maintenance or repair under voltage is inevitable it shall only be carried out by a skilled person who is aware of the hazard involved.

Note that capacitors inside the equipment may still be charged when the equipment has been disconnected from the supply. Before carrying out any work inside the equipment, capacitors connected to high voltage points should be discharged; to discharge mains filter capacitors, if fitted, short together the L (live) and N (neutral) pins of the mains plug.

Mains plug

The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action shall not be negated by the use of an extension lead without protective conductor. Any interruption of the protective conductor inside or outside the equipment is likely to make the equipment dangerous.

Fuses

Note that there is a 2.5 A circuit breaker in both the live and neutral wires of the supply lead. If only one of these breakers should trip, certain parts of the equipment could remain at supply potential.

To provide protection against breakdown of the supply lead, its connectors, and filter where fitted, an external supply fuse (e.g. fitted in the connecting plug) should be used in the live lead. The fuse should have a continuous rating not exceeding 6 A.*

Make sure that only fuses with the required rated current and of the specified type are used for replacement. The use of mended fuses and the short-circuiting of fuse holders shall be avoided.

* In the absence of a slow-blow fuse of this rating a higher rated e.g. 13 A, quick blow type may be used.

RADIO FREQUENCY INTERFERENCE

This equipment conforms with the requirements of IEC Directive 76/889 as to limits of r.f. interference.

CAUTION : STATIC SENSITIVE COMPONENTS

Components identified with the symbol on the circuit diagrams and/or parts lists are static sensitive devices. The presence of such devices is also indicated in the equipment by orange discs, flags or labels bearing the same symbol. Certain handling precautions must be observed to prevent these components being permanently damaged by static charges or fast surges.

(1) If a printed board containing static sensitive components (as indicated by a warning disc or flag) is removed, it must be temporarily stored in a conductive plastic bag.

(2) If a static sensitive component is to be removed or replaced the following anti-static equipment must be used.

A work bench with an earthed conductive surface.

Metallic tools earthed either permanently or by repeated discharges.

A low-voltage earthed soldering iron.

An earthed wrist strap and a conductive earthed seat cover for the operator, whose outer clothing must not be of man-made fibre.

(3) As a general precaution, avoid touching the leads of a static sensitive component. When handling a new one, leave it in its conducting mount until it is required for use.

WARNING : HANDLING HAZARDS

This equipment is formed from metal pressings and although every endeavour has been made to remove sharp points and edges care should be taken, particularly when servicing the equipment, to avoid minor cuts.

WARNING : TOXIC HAZARD

Many of the electronic components used in this equipment employ resins and other chemicals which give off toxic fumes on incineration. Appropriate precautions should therefore be taken in the disposal of these items.

Beryllia (beryllium oxide) is used in the construction of the following components in this equipment :

Unit AB2 : Transistors TR23 and TR26

This material, when in the form of fine dust or vapour and inhaled into the lungs, can cause a respiratory disease. In its solid form, as used here, it can be handled quite safely although it is prudent to avoid handling conditions which promote dust formation by surface abrasion.

Because of this hazard you are advised to be very careful in removing and disposing of these components. Do not put them in the general industrial or domestic waste or despatch them by post. They must be separately and securely packed and clearly identified to show the nature of the hazard and then disposed of in a safe manner by an authorized toxic waste contractor.

Chapter 4-1

BRIEF TECHNICAL DESCRIPTION

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1 Introduction
2 Circuit summary
2 Frequency generation
6 Counter/synchronizer
7 Modulation processing
8 Output processing
11 Microprocessor control

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INTRODUCTION

1. The following summary is an outline circuit description of the instrument and is intended to be read in conjunction with the block diagram. Detailed descriptions of each stage are given in Chap. 4-2.

CIRCUIT SUMMARY

Frequency generation

2. The 2017 utilizes one foreshortened coaxial line low noise oscillator covering the range 256 to 512 MHz from which all other carrier frequencies are derived. Frequencies from 4 MHz to 256 MHz are obtained by successive division by two in a total of six ranges. Frequencies from 10 kHz to 4 MHz are obtained by a mixing process derived from the 4 to 8 MHz range.

3. 4 MHz to 512 MHz. The low noise master oscillator covers a frequency range of 256 MHz to 512 MHz. Frequencies from 4 MHz to 256 MHz are obtained by dividing down the master oscillator range with six successive divide-by-two networks.

4. 512 MHz to 1024 MHz. The master oscillator frequency is utilized to phase lock one of two voltage controlled oscillators which together cover the range 512 MHz to 1024 MHz. This enables the low noise properties of the master oscillator to be transferred to this frequency range.

5. 10 kHz to 4 MHz. The lowest frequency range derived by division of the master oscillator frequency is 4 to 8 MHz. This is mixed with a 31.5 MHz crystal oscillator to produce a signal frequency in the range 35.5 to 39.5 MHz. Unwanted mixer products are then removed by a surface acoustic wave (SAW) band-pass filter. The signal is then further mixed with the output of a 35.5 MHz LC oscillator to produce an output in the range 10 kHz to 4 MHz. The crystal oscillator and the LC oscillator are phase locked to maintain an exact 4 MHz frequency difference.

Counter/synchronizer

6. The carrier frequency is indicated by a frequency counter in the unlocked mode. Greater stability can then be achieved by the locking process. This is a synchronized mode of operation, selecting the displayed output frequency and locking this to a high stability internal reference oscillator. Control of the master oscillator motor drive is also via the counter/synchronizer circuits providing the frequency selection and sweep facility.

Modulation processing

7. The a.m. and f.m. drive to the modulators may be derived from either an internal oscillator or an external source. Selection of modulation depth, deviation or internal oscillator is carried out on the front panel or by a programmable source. On selection of AM or Pulse Mod the signal is passed through a double balanced mixer type modulator. When FM is selected the modulation is achieved by a varactor located in the master oscillator tuned circuit.

Output processing

8. Two output amplifiers are utilized, both incorporating automatic level control. The first covers the frequency range 10 kHz to 4 MHz and the second 4 MHz to 1024 MHz. The second amplifier has additional fine level control and output level error correction required for the higher frequencies.

9. Outputs from the amplifiers are up to 4 V e.m.f. in c.w. and f.m. modes, (2 V e.m.f. for a.m.). This output is controlled by attenuator circuits to give selected level outputs of between 0.2 μV e.m.f. and 4 V e.m.f. in 0.1 dBμV steps. The amount of attenuation can be selected manually by either the r.f. level COARSE and FINE controls or entered via the keyboard. Alternatively selection can be made by a remote programmed source.

10. The final stage of the 2017 incorporates a reverse power protection. This is a safeguard to protect against possible damage to the attenuator unit by the accidental use of a transceiver's transmit mode and will protect the output attenuators against these unwanted reverse power levels for up to 50 watts.

Microprocessor control

11. Functions of the 2017 are controlled by the manual front panel controls or by entering the requirement on the keyboard and consequently the microprocessor, see Fig. 2 below. Alternative remote control is made easy by the GPIB interface also fitted to the 2017.

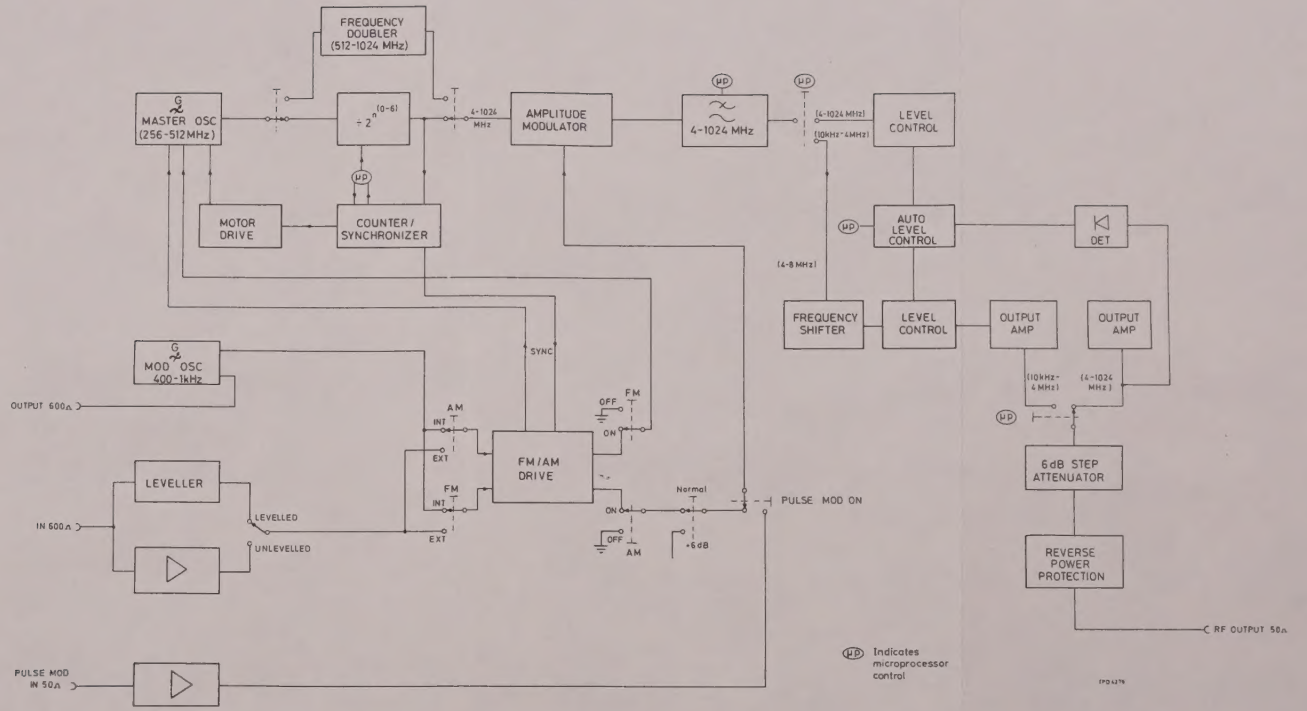

Fig. 1 2017 Simplified block diagram

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MASTER OSCILLATOR (AS1)

Circuit diagram : Chap. 7, Fig. 22

1. Master oscillator AS1 is a foreshortened coaxial line low noise design covering the range 256 to 512 MHz, it comprises a grounded base transistor TR1, transformer coupled to a high Q tuned circuit. Main tuning is achieved by varying the capacitor loading on the $\frac{1}{4}\ \lambda$ line inductor either by the operation of an 11 turn manual front panel control or by a motor drive M1. End stop switches SBA, SBB take off the motor supply when the extreme clockwise or counter-clockwise position of the tuning capacitor is reached.

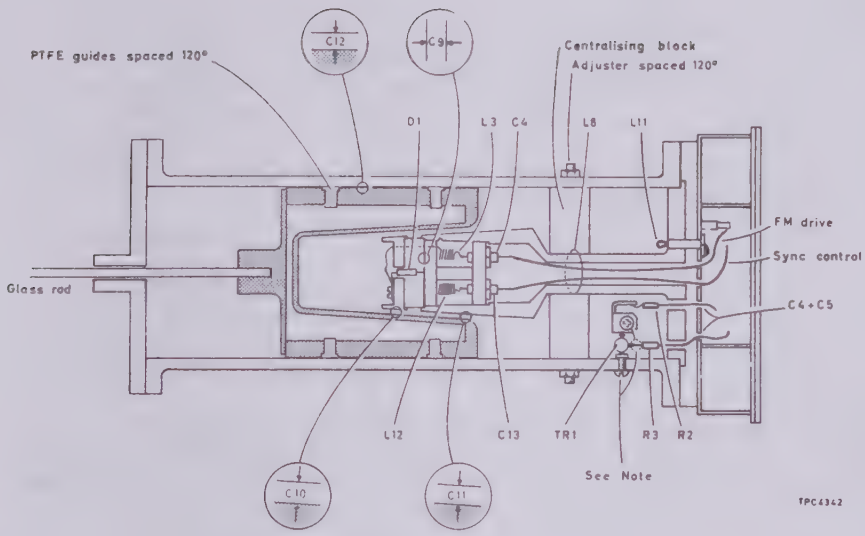
2. Individual components within the master oscillator are illustrated in Fig. 1. From this it can be seen that the varactor D1 couples in a further section of core, this has the effect of changing the tuned circuit capacitance and provides the means of applying frequency modulation and the electrical fine tune signal from the synchronizer. Manual fine tuning is carried out by a $3\frac{3}{4}$ turn front panel control providing 0 to ±8 V d.c. varactor bias voltage derived via board AS5.

3. Potentiometer R1 provides the filter section AA31 and range 9 VCO's with changeover information at the geometric mean of the frequency range of the master oscillator (355 MHz). It also provides the range 9 phase lock loop with coarse steering information.

4. The +12 V supply to TR1 collector, -0.7 V emitter supply, and the two signal voltages, to the FM on pin 6, and the electrical fine tune on pin 7, are all carefully screened to avoid spurious r.f. leakage.

Note...

No attempt should be made to solder any of the electrodes of TR1 otherwise damage to the transistor will result. Electrical contact is made by tightening the three securing screws shown until a good connection is made.



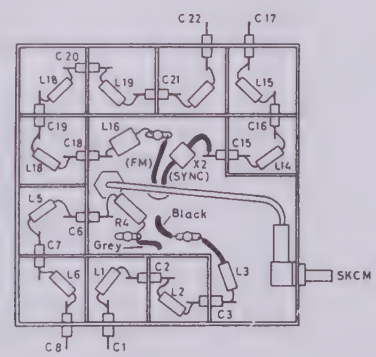


Fig. 1 Master oscillator (AS1)

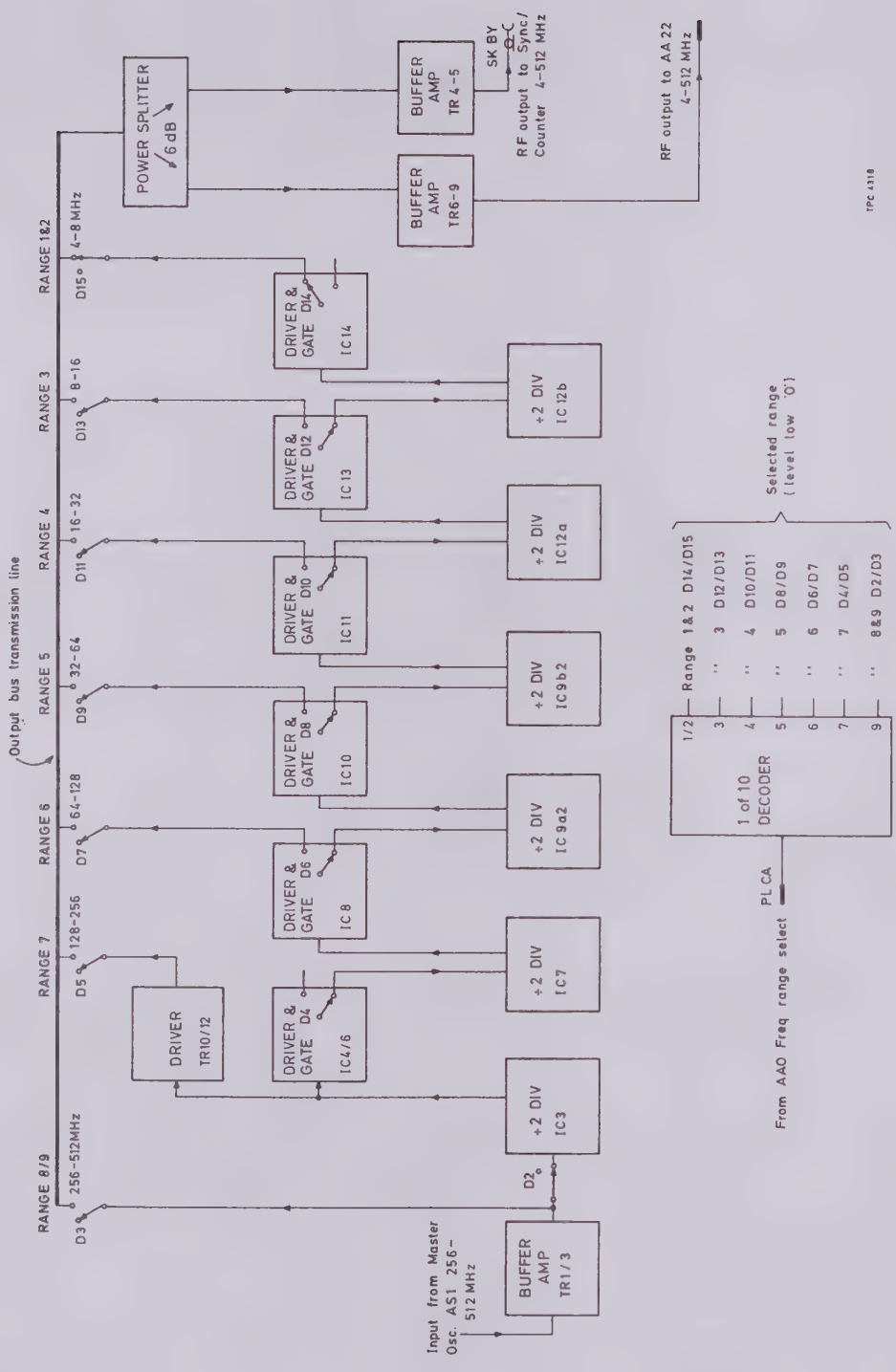


Fig. 2 Divider chain (AA11) simplified block diagram (with range 2 selected)

DIVIDER CHAIN (AA11)

Circuit diagram : Chap. 7, Fig. 15

5. The 256 to 512 MHz signal from the Master Oscillator unit AS1 is routed through unit AA11. TR1, TR2 and TR3 act as a buffer amplifier stage providing approximately 3 dB forward gain. Signals in ranges 8 and 9, that is 256-512 MHz, are connected directly to the output bus transmission line via D3 and are unaffected by the divider network. The seven remaining ranges pass through the relevant number of divider stages before being coupled to the output bus.

6. Output divider of the selected range only is coupled to the output bus and all others are uncoupled by the action of a gating circuit ensuring that dividers not required remain 'quiet' although powered.

7. The gating circuits are controlled by the TTL outputs from IC1, these are converted to ECL levels by resistor/diode networks e.g. R35, R36, R33 and D6. The gates are connected so that, when the signal from the divider is coupled to the output transformer, the signal used for driving the following divider is uncoupled.

8. Dividers are IC3, 7, 9a, 9b, 12a and 12b; gating circuits are IC6, 8, 10, 11, 13 and 14, and the output bus transformer coupling is carried out by diodes D5, 7, 9, 11, 13 and 15.

9. The output bus signal is then connected through the power splitter to two amplifiers. The synchronizer/counter buffer amplifier TR4, TR5 gives 0 dB forward gain and high backloss, and has its supplies isolated to prevent unwanted synchronizer signals being fed into the main signal path.

10. The second output buffer amplifier comprising TR6-TR9 provides the high output signal level required by the amplitude modulator on board AA21. Voltage/current feedback ensures a 10 dB gain, flat between 4 and 512 MHz.

RF SUB-UNIT 'A' (AA22)

Circuit diagram : Chap. 7, Fig. 17

Frequency doubler circuit

11. AA22 operates in conjunction with circuitry on AA21 to provide the Range 9, 512-1024 MHz signals. The 256-512 MHz signal from AS1 Master Oscillator fed via AA11 is phase locked to one of two varactor controlled oscillators (VCOs) which cover the frequency range 512-1024 MHz. Both signals are fed to a phase detector AA25 whose output controls the VCO frequency in a phase locked loop circuit. Selection of the required VCO is carried out by switching the supply rail which also has the effect of turning on the appropriate output diode D5 or D7 thus routeing the signal to the buffer amplifier TR1-3.

12. VCO selection is carried out by the Low/$\overline{\text{High}}$ instruction at the geometric mean of the master oscillator frequency (for details see AS7 technical description). The VCO is steered to a frequency approximately double the input frequency by the varactor diode control voltage. This is derived from the steering potentiometer RV1 linked to the master oscillator gear box. Steering potentiometer voltage initiates two different ramp outputs, one for each VCO (see AS7 technical description). These are fed from AS7 as the VCO

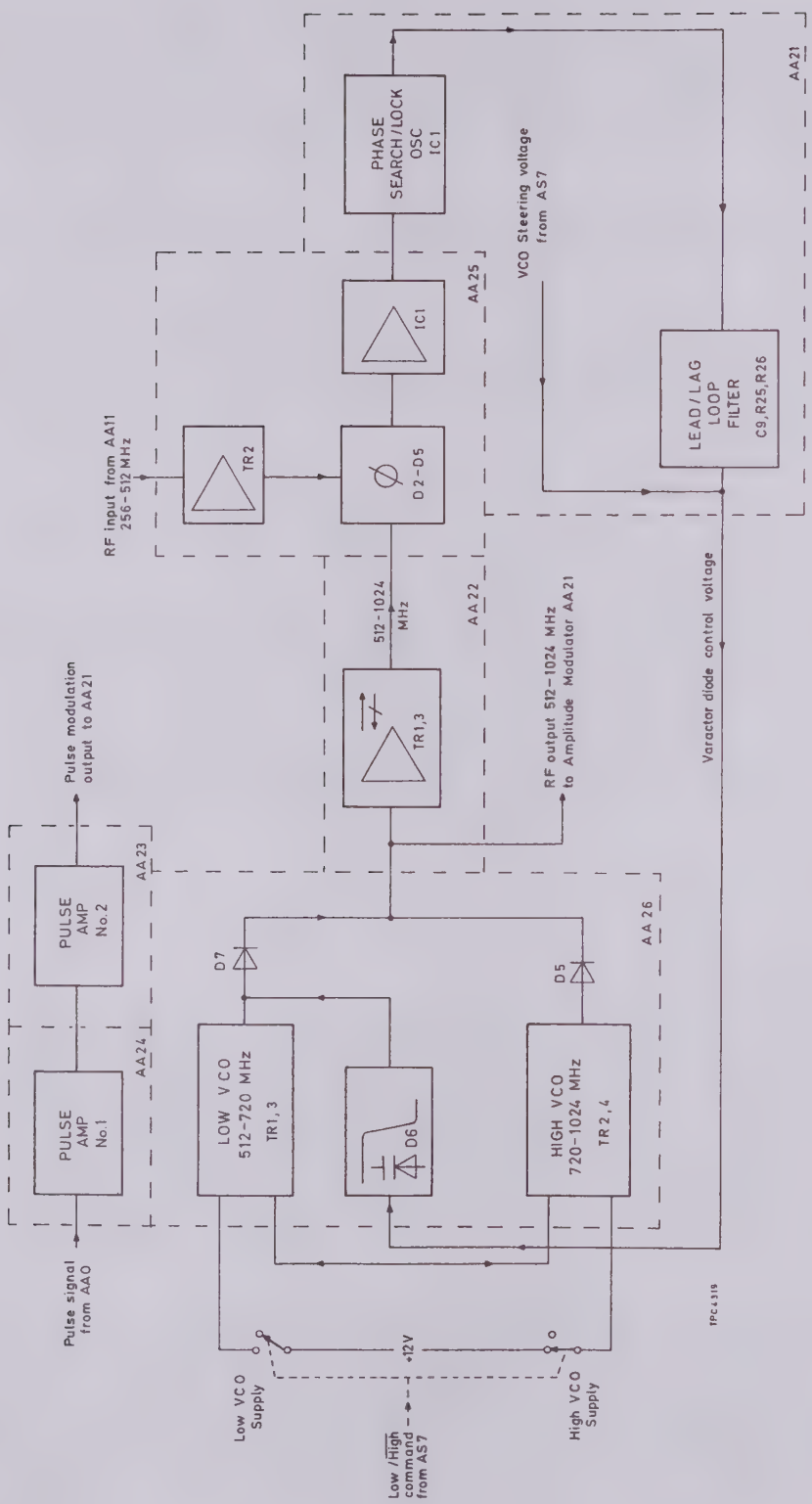


Fig. 3 RF Sub-unit 'A' (Frequency doubler) simplified block diagram (AA22)

steering voltage to be summed with the output of a search oscillator in the phase lock loop, formed by IC1 AA21 and its associated Wien bridge network.

13. The output of IC1 subsequently provides a swept varactor diode control to sweep not the entire frequency band but only a limited range near to the required fundamental frequency. Phase locking will then occur and the search oscillation ceases. The Wien bridge search oscillator is shown in Fig. 4. C5, C6, R9, R10 form the frequency dependent network and R8, R12 set the gain. When out of phase, point A appears to be at low impedance so that the gain of AA21 IC1 is $\frac{R8 + R12}{R12}$ which is >3. This satisfies the oscillatory condition for a Wien bridge circuit. When phase lock occurs, point A opposes movement of point B and so appears to be at high impedance. IC1 gain becomes $\frac{R8}{R12}$ which is <3, this prevents further oscillation and IC1 reverts to a straight amplifier. Typical lock and search varactor diode control voltages are as follows:

	Locked	*Search*
(i)	6.5 V	9.1 V / 4.0 V
(ii)	4.3 V	6.9 V / 1.7 V
(iii)	2 V	4.5 V / -0.6 V

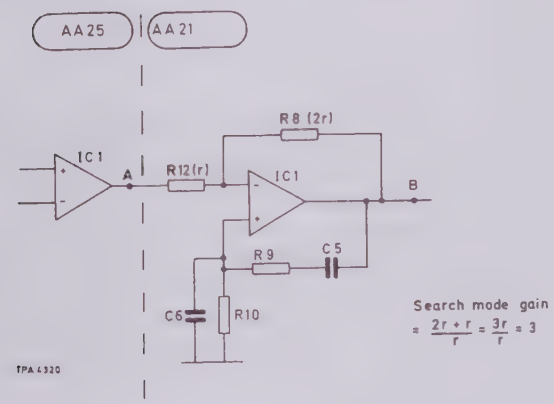


Fig. 4 Phase lock loop amplifier (AA25/AA21)

Pulse amplifiers (AA23, AA24)

14. These are described in the amplitude modulator AA21 circuit description.

AMPLITUDE MODULATOR (AA21)

Circuit diagram : Chap. 7, Fig. 16

15. Conventional amplitude modulation with depths variable from 0-99%, and pulse modulation are both obtainable in 2017. Two balanced mixers in cascade provide the modulation. The second, X2, carries out most of the modulation at low modulation depths. The first, X1, has a sufficiently large bias current to turn the diodes well on until large negative excursions of the audio waveform turn them off. Thus the first mixer deepens the troughs at high modulation depths, and the pair give ample carrier rejection for pulse modulation. Gain is achieved by a series of 5 dB amplifier stages; these each have a combination of shunt and series feedback to give flat gain to 1024 MHz with the minimum of adjustment.

Double balanced mixer stage

16. RF input to the first mixer stage is via SKCB or SKCC. Mixer X1 is driven with five times greater bias and audio current than mixer X2 as shown in Fig. 5. TR22 emitter follower gives a low distortion a.f. input to the i.f. port and also helps to alleviate possible diode junction non-linearity. The two stage amplifier TR15,16 TR20,21 boosts the signal to around 400 mV to feed mixer X2 ensuring sufficient drive and low distortion.

Audio signal processing

17. Two sources of audio signal may be used, the internal modulation oscillator or an external generator via the 600 Ω front panel input socket. These signals are passed through the modulation leveller board AS3 (either unlevelled or levelled) which outputs a 2 V r.m.s. signal. Incremental selection is obtained by an 8 bit digital-to-analogue converter, board AS4, the output of which, when 1 V r.m.s., represents 100% a.m. The a.f. signal bias current is then fed to board AA21 op-amp IC2, via the r.f. box AA22 where a 600 Ω audio filter prevents r.f. leakage. R62 sets the bias current for the mixers and final setting of gain. Audio gain can also be adjusted on the D/A board AS4 by R25.

18. When r.f. output levels in the range 2 to 4 V e.m.f. are selected (i.e. peak output) the bias current is doubled by switching on TR23 allowing the mixers to pass an extra 6 dB of signal. In this mode a.m. is not possible.

Pulse processing

19. RF screening of the pulse input front panel socket is carried out by two amplifier boards AA23, AA24, contained in the screened enclosure of board AA22. These present a high back-loss to r.f. signals whilst still providing sufficient bandwidth to avoid distorting the incoming pulses. R3, AA23 sets the d.c. output offset of these amplifiers and is adjusted so that with zero input, the mixers are turned completely off. The pulses can be overridden by a TTL instruction applied to AA24 pin 3. The pulse amplifiers then provide a peak d.c. level, used by the ALC system for pulse mode levelling.

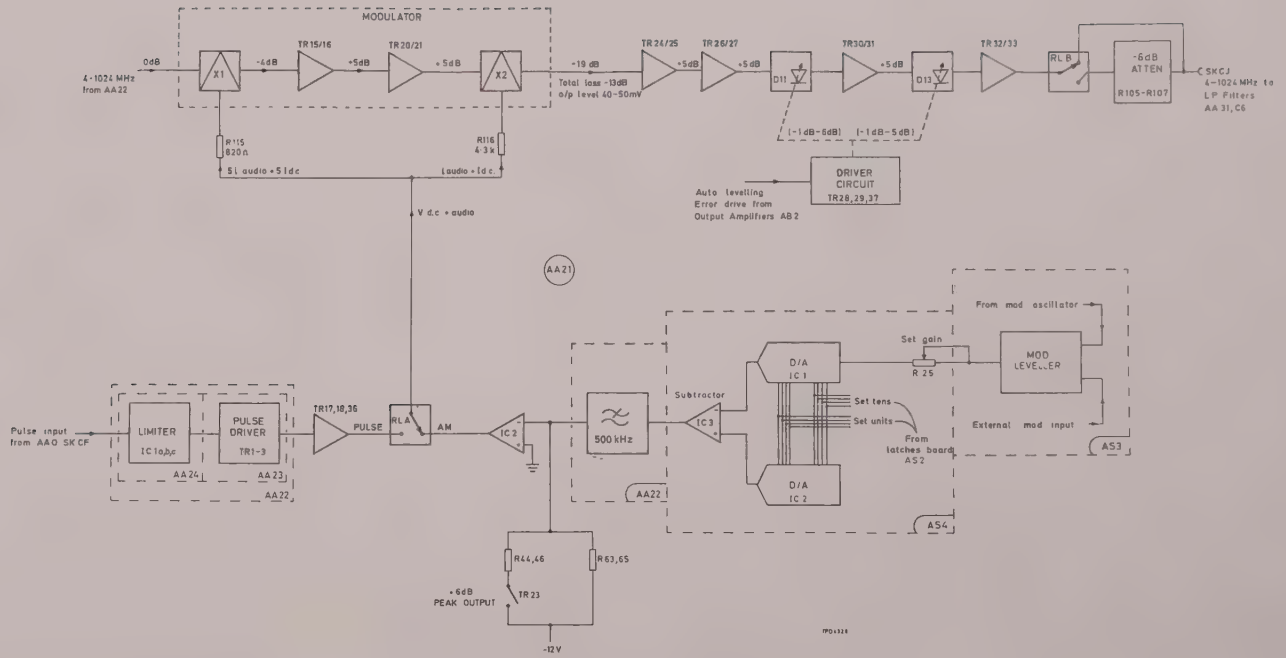


Fig. 5 Modulator unit (AA21) simplified block diagram

22. When AA21 TR5 turns on, current is drawn through the diode switching lines A, B, D and AA21 R1, turning on AA22 diodes D2, D4 and AA21, D1. AA22 diodes D1, D3, D5 and AA21, D2 are turned off allowing the Ranges 1-8 signals (4-512 MHz) at SKBZ to pass via C18 through SKCB to AA21 modulator X1. When Range 9 ON is asserted 'high' at AA21 PLCE pin 5, TR1, TR3 and TR4 are turned on and TR5 is turned off; current flow is now from AA21 TR4, through diode switching lines A, B, C and D. AA22 diodes D1, D3, D5 and AA21 D2 are turned on. AA22 diodes D2, D4 and AA21 D1 are turned off. The Range 9 input signal (256-512 MHz) at SKBZ is then routed via AA22 D1 to the phase detector AA25 to be compared with the VCO signal. Output on Range 9 is taken from the AA26 VCO output. PLCC (512-1024 MHz) to AA21 SKCC, C2 and D2 to modulator X1, current flow and signal path are illustrated in Fig. 6. The three stages of diode switching used in this circuit, each isolated in its own screened box, are designed in this manner to provide isolation of unwanted sub-harmonic when Range 9 is on.

23. On selecting Range 9 TR3, TR8 and TR11 are all turned on. The low/$\overline{\text{high}}$ instruction originated on board AS7 is fed to the bases of TR9 and TR12. On asserting 'low' TR9 and TR10 turn on and +12 V low VCO supply is fed through TR11 and TR10 to AA22. When '$\overline{\text{high}}$' is asserted TR9 and TR10 turn off and TR12 turns on connecting +12 V high VCO supply through TR11 and TR12 to AA22. TR13 and TR14, also connected to the high VCO line, are turned on to connect R37 to the search oscillators lead/lag filter C9/R25/R26.

24. Search oscillator on/off control. One further function of the Range 9 ON instruction is to turn both TR7 and TR6 off allowing the search oscillator IC1 to operate. When Ranges 1-8 are selected TR7 and TR6 are turned on and IC1 is disabled by earthing pin 3.

LOW-PASS FILTERS (AA31)

Circuit diagram : Chap. 7, Fig. 18

25. The function of this board is to filter and therefore reduce the harmonic content of the signal produced at the output of the amplitude modulator AA21. Each octave frequency range from 4 MHz to 1024 MHz requires two low-pass filters. This results in a total of 16 filters of which only one is in use at any given frequency. Range 1, 10 kHz to 4 MHz, does not require separate low-pass filtering.

26. The use of two filters per range, i.e. upper and lower half octave, is necessary to satisfactorily reduce the second harmonic of the lower half octave signal, see Fig. 7.

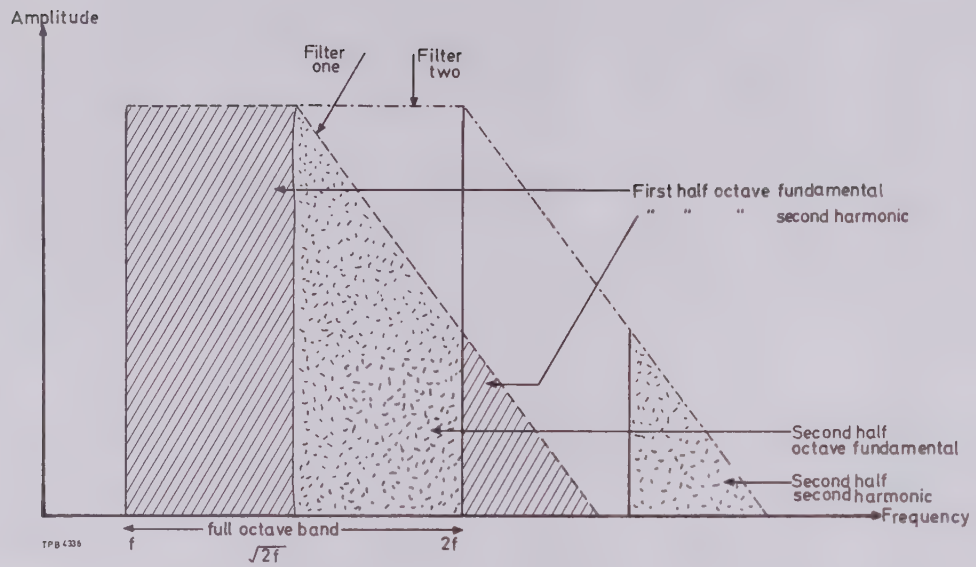


Fig. 7 First and second half octave filter characteristics (AA31)

Low-pass filters, circuit description

27. PLCL pins 4, 5, 9 and 11 provide 4 bits of input data 1, 2, 4, 8 where the most significant bit is 8. This is driven by the inverted low, '$\overline{\text{high}}$' VCO changeover line which itself is derived from R1 on AS1.

28. If the selected frequency is in the upper half octave of any range PLCL pin 9 instruction is 'low', TR1 collector and IC1 pin 20 are 'high'. Output from IC1 will be 'low' on one of the eight pins 9 to 17 selecting the relevant filter from the upper bank, all other outputs remain 'high'.

29. Selection of a frequency in the lower half octave of any range gives a 'low' instruction at PLCL. TR1 collector and IC1 pin 20 voltage will be 'low' and the 'low' output from IC1 will be on one of the pins 1 to 8 selecting a filter from the lower bank.

30. Ranges 1 and 2, although selected initially by separate instructions to IC1, have the outputs combined by IC3 to use the same filters. Range 9 line is decoded separately by IC2 and a connection to TR1 collector enables either the upper or lower octave filter as appropriate. IC2 also disables range 8 filters when range 9 is selected.

31. Frequency input to the board is from PLCJ; R4, R5, R6 form a 6 dB matching attenuator, TR3 and TR5 each provide 5 dB gain. C15 couples the signal input to the 50 Ω filter input bus. Two output buses connect the filter outputs to C91, the upper half octave filters, ranges 1 to 8, operate via D51 and range 9 via D49. The lower half octave filters, ranges 1 to 8, operate via D52 and range 9 via D47. TR23 and TR25 provide a further 10 dB gain, R97 is selected to give the correct output level.

32. The filters are selected in the following manner : assume a frequency in the upper octave of range 2 has been selected. IC1 pin 10 and IC3b2 pin 11 outputs are low and TR7 is biased on through D6/R28 voltage off-set components. Voltage on TR7 collector rises to +12 V, current flows through R31,D7, the output bus, D51 and R88 to earth. Current also flows in parallel through L9, L10, D8, the input bus, and R23 to earth, effectively coupling the filter to the input and output bus. Filters not in use have the switching

diodes reverse biased by a standing -12 V applied to each switching transistor collector.

OUTPUT AMPLIFIERS AND ALC (AB2)

Circuit diagram : Chap. 7, Fig. 21

33. The function of board AB2 is to provide amplification to the maximum required output level and automatic level control. Signals from AA31 filter board (4-1024 MHz) are passed through the high frequency output amplifier stages TR15-TR26 to the output. Range 1 (10 kHz-4 MHz) signal path is from unit AB1, through the low noise three stage amplifier TR2-TR4 followed by a class A push-pull output amplifier TR6-TR12. Operation of the ALC maintains an accurate output level and an effective source impedance of 50 Ω.

High frequency amplifier circuit description (4-1024 MHz)

34. Input from the filter board AA31 is passed through steering diode D27 to +5 dB amplifier TR15 and then to diodes D3 to D7 linear level controller. This controls the carrier amplitude in direct response to given microprocessor level instructions. R56 is adjusted in conjunction with R137 for linearity. TR18 and TR22 provide a further two +5 dB gain stages, R74 adjusts the level and R96 sets TR22 Ic for the least carrier distortion. L9, C42, R76 forms a low Q tuned circuit at 3.8 MHz and provides compensation for high-pass effects caused by the numerous .039 µF coupling capacitors used within AB2.

35. The final stages of amplification are carried out by two stud transistors TR23, TR26, both these contain beryllia (see Notes and Cautions). TR23 current driver stage is supplied by the +12 V rail and draws approximately 135 mA d.c. TR26 is supplied by the +22 V rail and the current adjusted by R100 for 200 mA d.c. C64 couples the output to T1 step up transformer and R108 output 50 Ω source resistor. Connection to the output socket is made through relay RLA, attenuator AT0 and the reverse power protection (r.p.p.) circuit.

Low frequency amplifier circuit description (10 kHz-4 MHz)

36. The lowest divided range signal from AA31 (4-8 MHz) is passed through steering diode D2 and out via SKCP to be processed by unit AB1, after processing the signal now in the range 10 kHz-4 MHz is re-entered via PLCX pin 7 from where it is fed to the low noise three stage amplifier TR2, 3, 4. The amplifier is used to provide the variable output level in direct response to given microprocessor level instructions. FET TR1b operates as a d.c. controlled variable resistance in the amplifier's feedback. Its control voltage is produced by a d.c. mimic circuit TR1a, IC1, IC2 in which the gain of IC1 is identical to the gain needed in the signal amplifier TR2-4. Integrating comparator IC2 produces the gate drive voltage for the matched f.e.t's TR1a, b. The reference voltage across R2, amplified by IC1, is held equal to the level instruction voltage across R111.

37. TR5 normally applies 6 dB attenuation which is removed when an instruction for full output is made. TR6 to TR12 form a class A push-pull amplifier. Connection to the output socket is made through R37 source resistor, relay RLA, attenuator AT0, and the reverse power protection in common with the high frequency signal path.

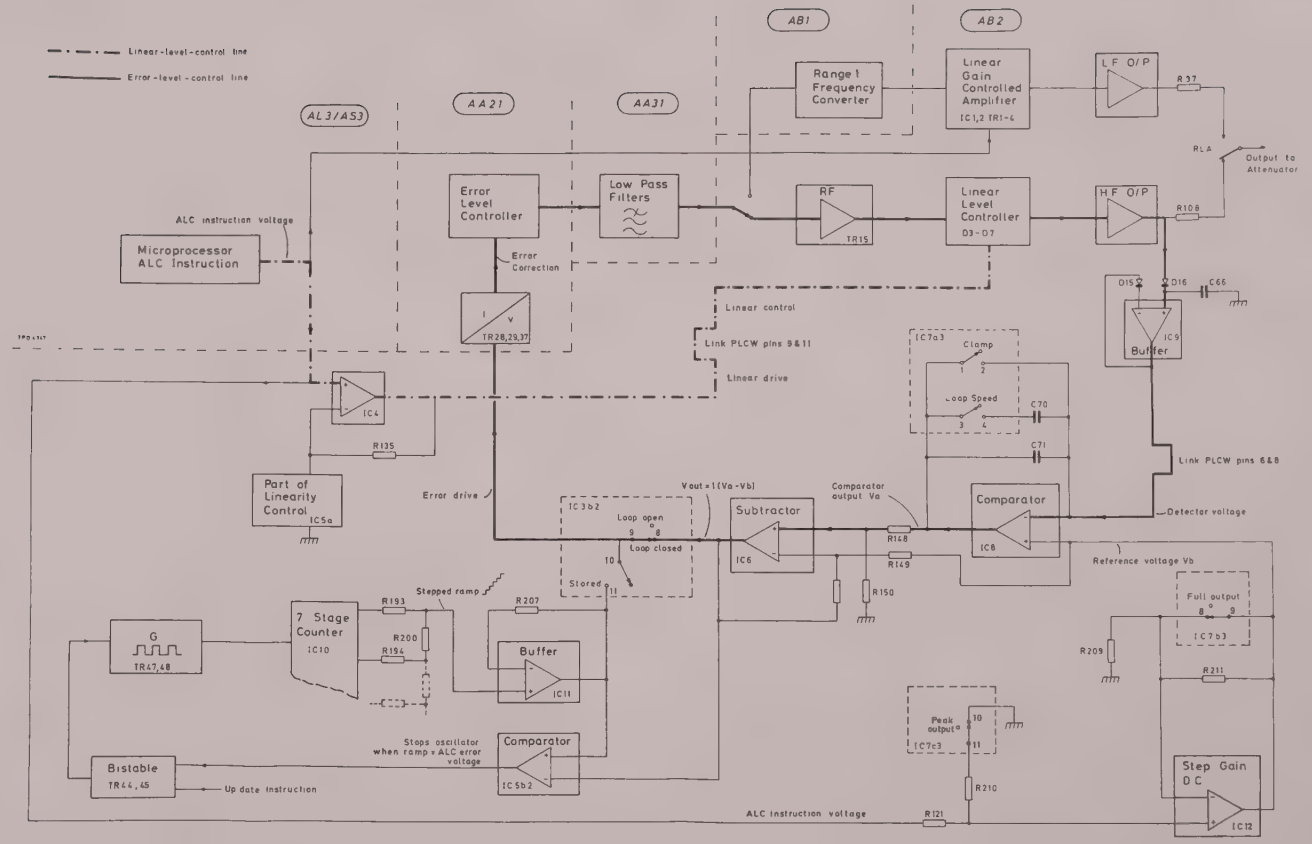


Fig. 8 Output amplifiers and ALC, (AB2) simplified block diagram

ALC operation

38. The purpose of the ALC circuit is to maintain an accurate output level and source impedance of 50 Ω at the output despite changes in the amplifier's output load impedance. A highly linear detector monitors the signal level at the junction of T1/R108 and its d.c. output is compared with a reference voltage to provide automatic level correction. Further refinements include a linear level control directly driven by the reference voltage which ensures rapid level adjustment to approximately the correct level before the slower integrating feedback loop takes effect.

39. An ALC store circuit is also incorporated, and is brought into circuit whenever Pulse Modulation or VOR/ILS a.m. is selected. The ALC loop is open circuited and an alternative loop correction voltage is applied, derived from a digital store. If the operating frequency of the generator is changed by a significant amount an update sequence operates to readjust the level of the stored voltage so maintaining the level accuracy.

ALC circuit description

40. Linear-level-control. When an r.f. level is selected the microprocessor gives an appropriate ALC instruction (between +1 V to +2 V) to board AB2, PLCW pin 16, and from there to pin 3 of buffer amplifier IC4. Output of IC4 is connected via IC5a to the linear drive line, through a link across PLCW pins 9 and 11, along the linear control line through D10, L7, L6 to the linear-level-controller D3-D7. IC5a improves the linearity of D3-D7. The linear-level-controller provides an immediate approximation of the required level, the slower acting error-level-control feedback loop then correcting any level inaccuracies.

41. Error-level-control. Changes in level are sensed by D16, a Schottky diode which is forward biased at 4 μA by R160 and buffered by op. amp. IC9. The temperature dependent voltage drop of D16 is exactly compensated for by matched diode D15.

42. The detector voltage at the output of IC9, a positive-going d.c., is compared with a reference voltage Vb (see Fig. 8) produced by the microprocessor via a D-A converter. Both signal voltages are fed to IC8 d.c. integrating comparator to produce an error voltage Va. IC9 detector voltage is fed via R77, R78 divide-by-two network, and through a link across pins 6 and 8 of PLCW (test socket). The ALC microprocessor instruction, between +1 V and +2 V from pin 16 of PLCW is fed to switched attenuator R210, R121, and IC12 programmable step gain d.c. amplifier. The gain of these may be switched to Normal x1, Full output x2, or Peak output x4.

43. In the Normal output condition (output voltages up to +120 dBμV e.m.f.) IC7b3 and IC7c3 contacts remain closed and unity gain results from IC12. Instructions to IC7b3 for Full output (c.w., f.m. and a.m. output voltages up to +126 dBμV e.m.f.) disconnect pin contacts 8 and 9 connecting R211 and R209 across IC12 to produce a gain of 6 dB.

44. Instructions for Peak output (c.w. and f.m. only, output voltages up to the maximum level +132 dBμV e.m.f.) disconnect IC7c3 pin contacts 10 and 11 to remove R210 from circuit and double the ALC instruction voltage fed to IC12 and hence give a further 6 dB output. R213 and similarly R159 and R151 adjust the input offset null on IC12, IC9 and IC8 respectively.

45. IC12 reference voltage (Vb, see simplified block diagram) is compared with the detector voltage from IC9 by the d.c. integrating comparator IC8. Output from the comparator, Va, is fed to IC6 operating as a subtractor. This removes from IC8 output the ALC reference voltage, Vb, leaving only the error drive voltage at the output of IC6, $V_{out} = 1\ (Va - Vb)$.

46. Unless Pulse Modulation or VOR/ILS a.m. is selected IC3b2 operates in the loop closed condition and the error drive is coupled to the error correction circuit on board AA21 via PLCW pin 5. Here TR28, 29, 37, voltage-to-current converter adjusts the current flow through D11, D13 and hence the r.f. level in all succeeding stages. The feedback loop settles at the error drive voltage which produces the r.f. output level selected, at which point the d.c. voltage from the output level monitor will exactly equal the ALC reference voltage, Vb.

47. TR38, TR39 provide two identical offset voltages to both inputs of IC8 so that its inputs and output are the same when the error drive voltage is in the centre of its working range. R153 allows the two offset voltages to be balanced.

ALC store

48. If either the Pulse Modulation or VOR/ILS a.m. modes of operation are in use the ALC loop is open circuited to avoid interfering with these types of modulation. The error drive voltage is then derived from a digital store via a D-A converter instead of the normal closed loop source. To prevent the opened ALC loop drifting to its limits it is held in the centre of its working range by a clamp circuit as shown in Fig. 9 below. If a significant change is made in the generator operating frequency an ALC update sequence operates to correct the stored voltage.

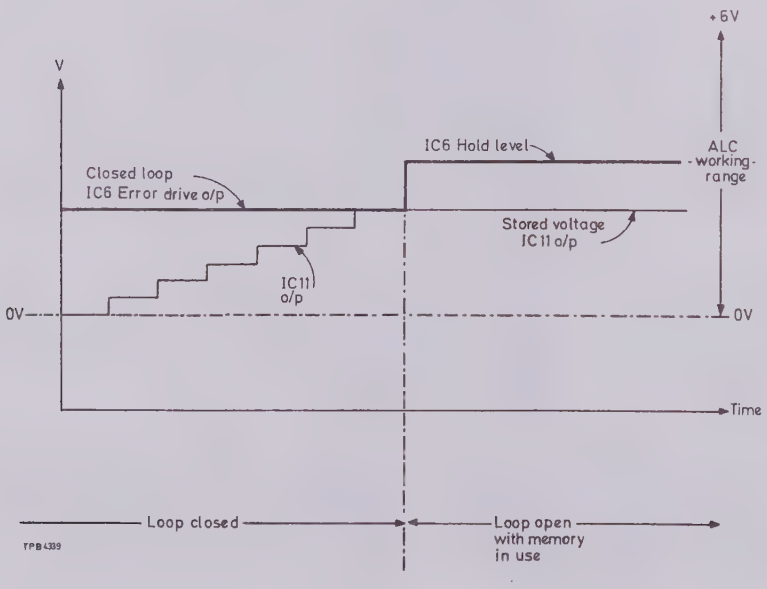


Fig. 9 ALC clamp operation (AB2)

49. ALC store, circuit description. The initial store operation takes place as soon as Pulse Modulation or VOR/ILS a.m. is selected. The feedback loop remains closed and modulation is inhibited for approximately 20 ms. The store circuits are controlled by a bistable TR44/TR45, together with the microprocessor lines "ALC continuous" and "ALC update". Transistors TR47/TR48 are coupled as an oscillator and, when enabled by the bistable, clock the seven stage counter IC10 previously reset via D24. This drives a D-A converter R193-R206 and buffer amplifier IC11. The output of IC11 is fed to comparator IC5b2 and increases in successive discrete steps, up to 128, until the voltage equals the error drive voltage on the other side of IC5b2.

50. When this occurs IC5b2 output sets the bistable (TR44 is turned on), preventing further oscillation from TR47/TR48. Switch IC3b2 operates via TR45 collector and pins 8 and 9 are disconnected to open the loop, also pins 10 and 11 are connected to couple the stored voltage to the error drive line and from there to board AA21. Switch IC7a3 is also operated via D19, pins 1-2 are connected together to clamp the input and output of comparator IC8. This holds the output of IC8 in the centre of the ALC working range throughout the time that the loop is in the open condition. Figs. 9 and 10 show this operation.

51. Update sequence. The microprocessor ALC update instruction is made if the frequency of the generator is changed by a significant amount. Modulation is inhibited and the ALC loop again closed for approximately 20 ms. The process begins when the microprocessor gives a 15 ms logic '1' instruction to the base of TR41 via PLCW pin 2. TR41 and TR43 cause the bistable circuit TR44/TR45 to reset via R177. Seven stage counter IC10 is reset at the same time via R173.

52. The previous stored voltage of IC11 is returned to 0 V and the oscillator TR47/TR48 is inhibited by TR46 via R181. Loop time constant is reduced by the removal of a capacitor C70, this is normally connected in parallel with C71 across the comparator IC8. Removing this from circuit allows the loop to settle in only a few ms to facilitate rapid memory update. This is initiated when TR42 collector goes 'low' and the switch IC7a3 open circuits pins 3 and 4.

53. On completion of the 15 ms ALC update instruction TR43 collector releases TR46 oscillator inhibit previously held via R181. This allows the oscillator to function which in turn allows the seven stage counter to be clocked, TR43 collector also releases the seven stage counter reset line via R173. The output of IC10 is fed to IC11 buffer amplifier through the D-A converter R193 to R206 giving a series of (up to 128) increasing discrete voltage steps on one input of comparator IC5b2.

54. When the stepped voltage equals that of the closed loop error drive voltage, IC5b2 output will again set the bistable to prevent further oscillation or counter output. Switches IC3b2 and IC7a3 operate as described previously in para. 50 to connect the updated stored voltage to board AA21 and maintain the hold level (clamp) voltage at IC6 output.

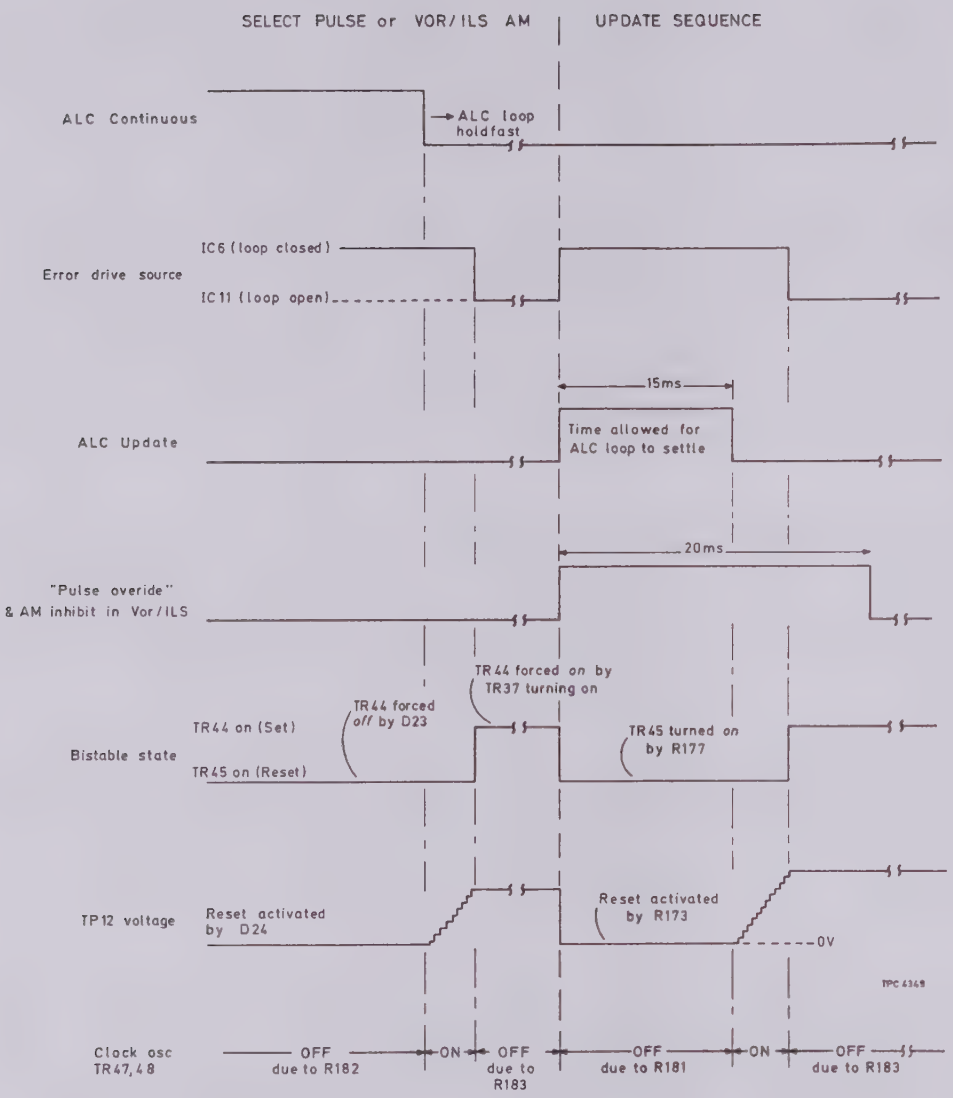


Fig. 10 ALC store and update operation (AB2)

Carrier off condition

55. If Pulse Modulation or VOR/ILS a.m. is selected whilst in the Carrier off mode the ALC loop is in the store condition and this fixes the memories' first record. When Carrier on is subsequently selected the stored ALC error drive voltage is invalid. This condition is corrected by the microprocessor initiating an update sequence.

10 KHZ-4 MHZ PROCESSING BOARD (AB1)

Circuit diagram : Chap. 7, Fig. 20

56. The function of this board is to provide from the last divided range of board AA11 frequencies in the range 10 kHz to 4 MHz. The input from board AA11 is first mixed with a fixed 31.5 MHz crystal oscillator. The frequency produced, 35.5 to 39.5 MHz, is then fed through a band-pass filter and further mixed with a 35.5 MHz signal from a low noise LC oscillator to obtain the 10 kHz to 4 MHz required.

57. To achieve an accurate and stable output, the two oscillator outputs are mixed to produce a 4 MHz signal which, when divided by four, is compared with a 1 MHz reference signal from the instrument's internal standard and finally phase locked to maintain a precise 4 MHz frequency difference. Any error is used to correct the 35.5 MHz LC oscillator frequency.

AB1 circuit description

58. Crystal controlled oscillator (TR2 and TR3). This has a resonant frequency of 31.5 MHz and includes a timed circuit in the collector of TR2 to suppress the third overtone of the crystal. TR4 amplifies and provides two outputs, one to signal mixer X1 via tuned circuit T1, C12, C34 (see (b) Fig.11 simplified block diagram) and the second via T1 coupling transformer secondary to the control mixer TR5.

59. Signal mixer X1. This is a high performance double balanced mixer and sums the 31.5 MHz fixed frequency from TR2, TR3 via amplifier TR4 and the variable 4-8 MHz input signal (a) from board AB2. Resistor R3 adjusts the signal level to X1 and TR1 amplifier drives X2 (35.5-39.5 MHz) surface acoustic wave filter. X2 selects the sum component from the signal mixer X1 output (c) and TR6 6 dB gain amplifier provides impedance matching for the filter output. TR7 and TR8 buffer the network and R38, C24, L14 compensate for losses in X2 which would otherwise be apparent at 40 MHz.

60. TR9 variable gain amplifier. Has its output level controlled by an instruction voltage from board AS3. This is the range one level reference and is adjusted for output level calibration. If the detected output level of TR9 differs from the reference voltage fed to IC4 then its output will adjust TR9 gain until such time that both inputs to IC4 are the same. A further output of IC4 is also coupled to board AS4 via TR15 to provide a visual (l.e.d.) indication of the voltage in case a malfunction occurs in the ALC line. This circuit is described in the section on AS4.

61. Signal mixer X3. R45, R46, R47 provide 6 dB of attenuation to ensure a 50 Ω source impedance to X3, another high performance double balanced mixer. The second input to this mixer is the 35.5 MHz signal (d) from TR13 amplifier and TR12 voltage controlled oscillator. The output of X3 (e) is filtered by L6, L7, C32, C33 to pass frequencies in the range 10 kHz to 4 MHz to the low frequency output amplifier board AB2. Further filtering is carried out on that board by L2, C20.

62. Phase lock loop. Frequency accuracy is maintained by a phase lock loop applied to the 35.5 MHz voltage controlled oscillator TR12. The output of TR12 (d) is passed by C56, C57, L8 and fed to gate 1 of TR5 which is a dual gate depletion type m.o.s. f.e.t. mixer. The second input to the mixer is from the crystal controlled 31.5 MHz oscillator TR2, TR3 (b) which is fed to

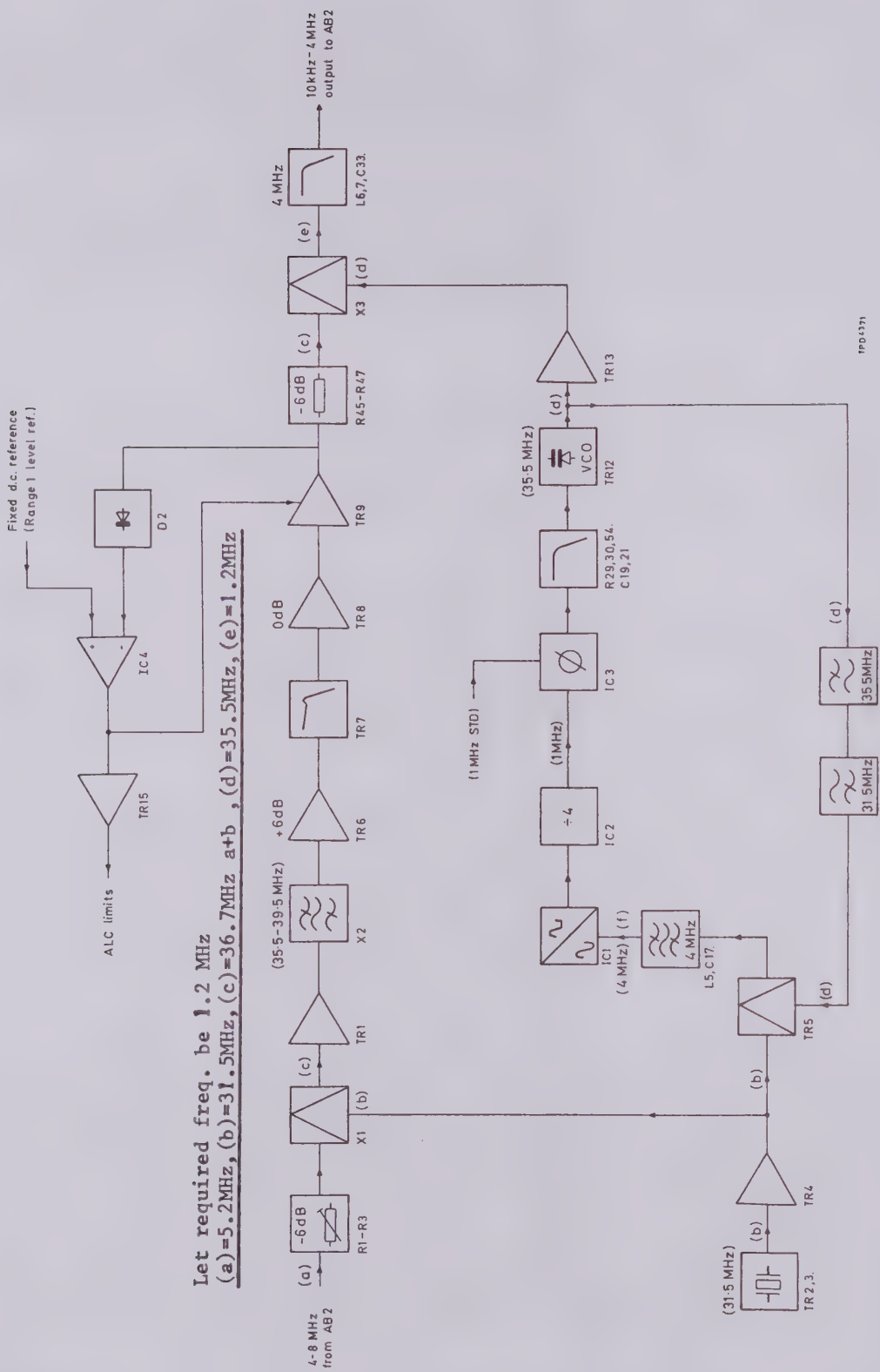


Fig. 11 10 kHz-4 MHz Range 1 processing (AB1) - simplified block diagram

gate 2 of TR5. The difference frequency output, 4 MHz (f), is selected by the output tuned circuit L5, C17 and fed to a limiting amplifier IC1 and a divide-by-four circuit IC2. The resultant 1 MHz signal is fed to one input of a phase comparator IC3. Comparison is made with the reference standard 1 MHz signal derived from the instrument standard on board AL4.

63. The phase comparator triggers on each low-to-high transition at the signal (pin 14) and comparator (pin 3) inputs. If the input frequency at pin 14 is higher than that at pin 3 the p-channel output at pin 13 is turned on to pull the output voltage positive. If the input frequency at pin 3 is higher than pin 14 the n-channel output at pin 13 is turned on to pull the output voltage negative. The resulting filtered voltage is applied to varactors D4, D5 to adjust the frequency of oscillator TR12. When an exact 1 MHz difference frequency is obtained at the comparator input, the p and n channels are then turned on only for a period of time corresponding to the phase difference until finally the output is decreased to zero output when both inputs are locked in phase.

64. TR12 is a voltage controlled Clapp oscillator with a series tuned tank as part of the total feedback network. An LC phase inversion is formed with C40 and C41. D4 and D5 varactors provide phase lock correction to the loop and TR13 forms a tuned amplifier to give the necessary matching to the second signal mixer X3.

RF OUTPUT LEVEL

65. Attenuation is carried out by a coarse 6 dB step attenuator and a 6 dB fine level control. Selection is carried out by either manual control or entered on the keyboard and is displayed in units of volts e.m.f. and p.d., dB relative to 1 µvolt e.m.f. and p.d. or dBm. The units are selected by means of a front panel switch.

Attenuator (AT0)

Circuit diagram : Chap. 7, Fig. 30

66. This is a coarse 6 dB step attenuator and contains π networks of one 6 dB pad, one 12 dB pad, one 24 dB pad and three 30 dB pads. Each pad is switched by a solenoid; for 132 dB of attenuation all relays would be de-energized as shown in the circuit diagram. Relays are selected as described in the section on AS4.

67. Partial screening is built between the input and output ends of the pads, and flags are positioned around the series resistors to improve the v.s.w.r. Pads are switched out of circuit by energizing the appropriate coil which is wound on a soft iron core. This in turn operates an armature to set the microswitches and remove the pad from circuit.

REVERSE POWER PROTECTION (ARO)

Circuit diagram : Chap. 7, Fig. 31

68. The connector between the attenuator unit and the output socket incorporates a coaxial protection relay. The r.f. signal is detected and fed to a trip circuit via a comparator. With normal operating signal levels the comparator threshold is not exceeded and the relay remains energized, i.e. contact closed. With an overload the comparator output changes state and de-energizes the relay, opening the contacts. An indication of this is shown on the front panel initially by a flashing RF OFF annunciator. If the cause of the overload is removed the relay can be reset by depressing the RF ON/OFF front panel key and instantly the relay is again reset and the RF OFF annunciator turns off. If the overload is still on, depressing the RF ON/OFF key will cause the RF OFF annunciator to assume a steady on condition for 4 seconds before again resuming flashing. Each succeeding attempt to reset will incur a further 4 second cycle. This delay is to allow time for any overheated attenuator resistors to recover, preventing resetting at too frequent intervals.

RPP control

69. When the 2017 is initially switched on, assuming that no overload is present a 'low' instruction from the microprocessor via the tripped/$\overline{\text{reset}}$ line is fed to the base of TR2 via C7. The negative transition of this pulse is sufficient to turn on TR2 which in turn latches +5 V to one side of the relay RLA.

70. The r.f. signal via PLCU is attenuated by potentiometer chain R21-R24 and is detected by the full wave rectifier D1-D4. This is across load resistor R2 and across D5 whose inherent capacity provides the detector reservoir capacitor in addition to limiting rectified output to a maximum of 10 V. R21-R23 provides a d.c. path giving protection against a possible inadvertent d.c. overload, the input voltage d.c. threshold is approximately ±3.5 V. IC1 is a unity gain single ended output amplifier.

71. IC2 comparator threshold level at TP1 is set to about 0.8 V by R9 so that with no or normal r.f. levels applied the comparator output at TP2 will be high and TR1 relay switch turned on. This completes an earth return to allow relay RLA to energize connecting the attenuator to the output socket. The same earth return path causes TR3 to turn on also, providing a holding path for TR2. TR4 also switches on and maintains a 'low' level instruction to the microprocessor.

72. The comparator threshold level corresponds to an overload threshold of 4.5 V r.m.s. at 1 MHz and is such that a continuous r.f. overload of ½ W is possible without trip-out.

Overload condition

73. When an overload occurs, the level exceeds the threshold voltage on pin 2 and IC2 output drops to almost 0 V, TR1 is turned off; the earth return path is then broken for RLA which de-energizes. At the same time TR3 and subsequently TR2 also turns off and the +5 V supply is removed from RLA and TR4 base, TR4 turns off and a level '1' instruction is fed to the microprocessor via pin 6.

74. De-energizing the relay RLA removes the overload condition from the signal generator circuits allowing the RPP detector input to return to a normal operating level. IC2 comparator output returns high and TR1 turns back on, however latch TR2 and TR3 remain off so that no energizing voltage appears across RLA, and relay contacts remain open.

75. A front panel indication that the r.f. output has been interrupted is given by the flashing of the RF OFF annunciator. Depressing the RF ON/OFF key causes the microprocessor to initiate a reset cycle with a '0' level to once again turn on TR2 latching +5 V to remake the relay as described previously. If the overload has been removed, relay contacts will remain closed. If the overload is still present the circuit will again trip and a 4 second delay cycle described in the previous paras. will operate before a further reset cycle is initiated by the microprocessor.

Fine level control (AS2/AS3)

Circuit diagrams : Chap. 7, Figs. 24 and 26

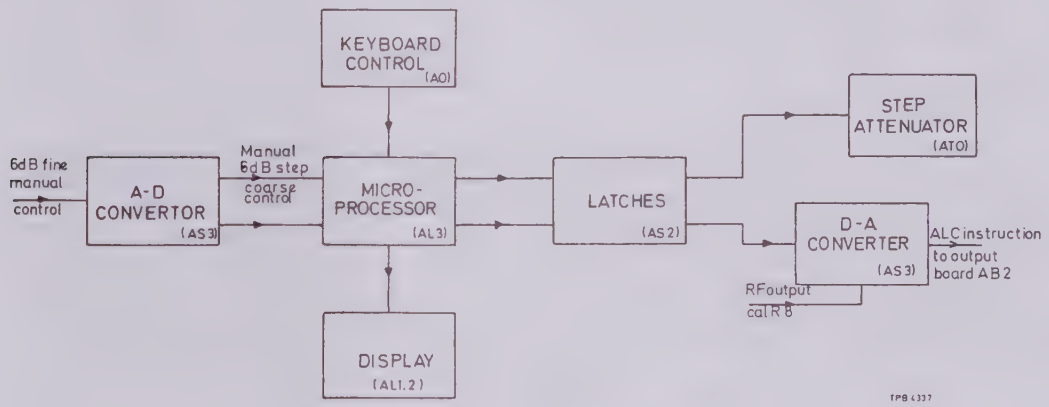


Fig. 12 RF output fine level control (AS2/AS3)

76. Fine level control is carried out over a nominal 6 dB range. When selection is made via the keyboard an instruction is passed direct to the microprocessor, this is processed and the digital information passed via the latches board to a D-A converter. The resulting voltage is used as an ALC instruction to control the output level of the signal amplifiers.

77. If selection is made from the variable front panel manual control, the voltage from this is first compared with a voltage ramp initiated by the microprocessor in an A-D converter. When the ramp equals the value of the fine level control voltage a measure of the time taken by the ramp is noted and an appropriate digital output is made by the microprocessor, see Fig. 13.

78. The digital information from the microprocessor is then processed as a keyboard instruction would be through the latches board and D-A converter to produce the ALC instruction. Details of both A-D and D-A converter operation are given in the section on AS3 modulation leveller board.

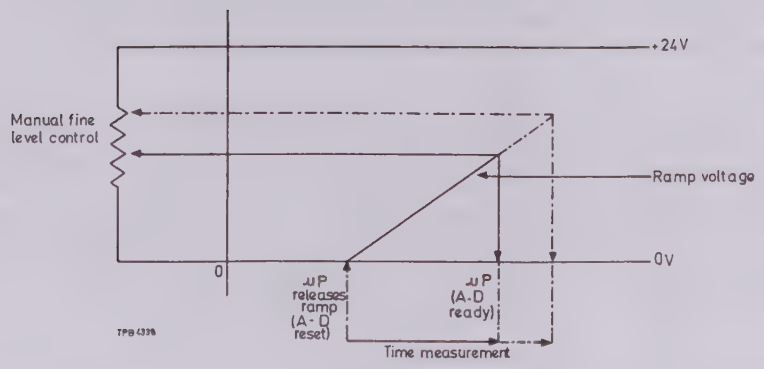


Fig. 13 Voltage/time converter (AL3/AS3)

AM AND ATTENUATOR CONTROL (AS4)

Circuit diagram : Chap. 7, Fig. 27

Attenuator control

79. Instructions from the keyboard or the manual coarse 6 dB step level control are processed by the microprocessor and an instruction via the latches board AS2 is passed to the a.m. and attenuation board AS4. Input is via plug PLBD on pins 11, 12, 13, N and P, a logic '1' causes one or more of the transistors TR2, 4, 6, 8 or 10 to turn on and consequently TR3, 5, 7, 9 or 11 are also turned on. Pads not required are then switched out of circuit by completing the earth return path from PLBP pin 4 through the turned on transistors. Logic selection for each 6 dB step from 0 to 132 dB is shown in Table 1.

TABLE 1 ATTENUATOR LOGIC (AS4)

Attenuation in 6 dB steps		*0*	*6*	*12*	*18*	*24*	*30*	*36*	*42*	*48*	*54*	*60*	*66*	*72*	*78*	*84*	*90*	*96*	*102*	*108*	*114*	*120*	*126*	*132*	*Pads out of circuit*
Data input to PLBD	4	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	60 dB
	0	1	1	0	0	1	1	1	0	0	1	1	1	0	0	1	1	1	0	0	1	1	0	0	12 dB
	1	1	1	1	1	1	1	0	1	0	0	0	1	1	1	1	1	0	1	0	0	0	0	0	30 dB
	2	1	0	1	0	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1	0	6 dB
	3	1	1	1	1	0	0	1	0	1	0	0	1	1	1	0	0	1	0	1	0	0	0	0	24 dB

Note...

Logic '1' applied to input 4 causes two 30 dB pads to be removed from circuit via pin 14.

AM control

80. The function of this circuit is described in board AA21 amplitude modulator circuit description.

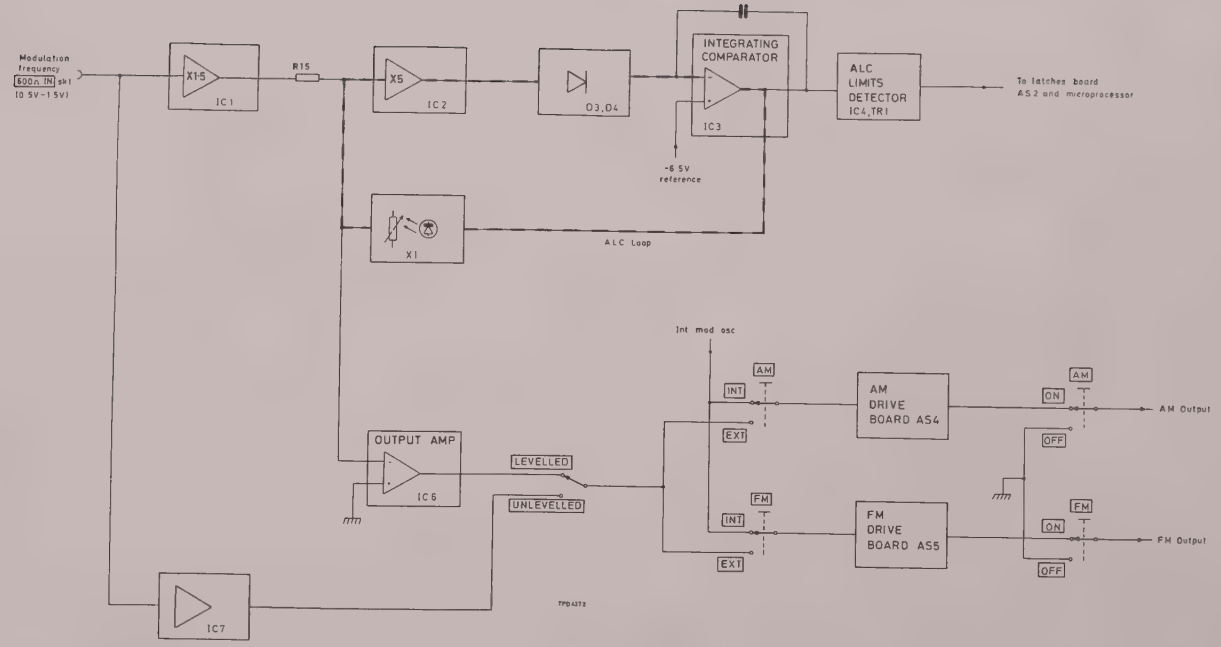


Fig. 14 Modulation leveller (external mod.) (AS3)

ALC limits detector

81. The ALC limits voltage, derived on board AB1 for range 1 and the error drive voltage derived on board AB2 for ranges 2-9, are both fed to analogue quad switch IC3a2 on board AB2. The voltage appropriate to the range selected is then connected to the ALC limits detector on AS4 board, pin 5. The circuit TR12-TR15 provides a visual indication should the ALC be inoperative or out-of-limits. It can only be seen within the confines of the instrument and is there as an aid to maintenance.

82. Upper limits circuit. If the ALC voltage is in excess of 6.2 V sufficient forward bias will be present to turn on both TR12 and TR14. Current drawn through TR14 will also turn on l.e.d. D2 to indicate that the r.f. output is too low.

83. Lower limits circuit. Whilst the ALC is within limits TR13 is turned on and the current drawn by TR13 is such that TR15 remains turned off. Only when the ALC voltage falls below 0.6 V does TR13 turn off, this allows TR15 and consequently l.e.d. D3 to turn on to indicate that the r.f. output is too high.

MODULATION LEVELLER (AS3)

Circuit diagram : Chap. 7, Fig. 26

Manual fine level A-D and D-A converter

84. The two converters are used in conjunction with the microprocessor to effect the manual 6 dB fine control of the r.f. output level, this is illustrated in the simplified block diagram Fig. 12 and the fine level control paragraph.

85. The microprocessor repeatedly updates the fine level attenuator control by releasing the A-D reset line at SKBB pin H. When this occurs TR2 is switched off and TR3 charges C21 to produce a positive-going voltage ramp at one input of the comparator IC8. The ramp continues until the voltage on IC8 pin 3 is the same as that on pin 2.

86. The input on pin 2 is derived from the setting of the manual front panel fine level control, this is connected to R1 and R2 between the +24 V rail and earth. When both the fine level wiper voltage and the ramp voltage are of the same value IC8 comparator output causes TR4 to conduct and output an A-D ready instruction '0' level to terminate a time counter within the microprocessor.

87. After processing, a digital notation is latched from the microprocessor back to board AS3, PLBB on pins 8-11 and J-M. Alternatively a fine level request from the keyboard would be processed directly by the microprocessor and latched to the same pins on AS3.

88. IC9 D-A converter is a monolithic 8-bit high speed current output D-A accepting TTL levels, R8 provides adjustment for output level calibration on ranges 2-9. IC10 with R55 converts the current to a positive-going, low impedance voltage output. The output (ALC instruction voltage) nominally between +1 V and +2 V is fed to board AB2 providing a reference voltage to enable the ALC circuit to set the correct output level.

Range one calibration

89. A level reference voltage derived from the wiper of R9 provides a fixed d.c. reference for range one r.f. output levels up to +126 dBμV. This reference is fed to the Range 1 processing board AB1 comparator IC4. When peak output is requested i.e. +132 dBμV a level '1' instruction from the microprocessor turns on TR5 and increases the reference level by a factor determined by the setting of R10, +6 dB cal. adjust.

Modulation leveller circuit (External mod) see Fig. 14

90. Unlevelled mode. External modulation input is via the front panel socket IN 600 Ω and is matched by R36 to the single amplifier stage IC7. This has a x2 gain adjusted by R5 to give 2 V r.m.s. output for a 1 V r.m.s. input. R4 adjusts the input offset voltage of IC7, and C25 provides h.f. compensation.

91. Levelled mode. All inputs between 0.5 V and 1.5 V r.m.s. are automatically levelled to give a constant 2 V r.m.s. output from this circuit. IC1, a low noise a.f. amplifier, d.c. coupled with a fixed x1.5 gain drives an electronic attenuator comprising R15, X1.

92. IC2, IC3, TR7 and R15,X1 form an ALC loop, a fixed reference on IC3 pin 3 d.c. integrating comparator (-6.5 V) is compared with the rectified output of amplifier IC2. This has a x5 gain to provide a large input signal to the detectors D3, D4. D1 and D2 in series with the feedback path fully compensate the temperature dependent off-set voltage of diodes D3 and D4. C26 compensates the low frequency detector response. C7, C9, D3 and D4 make up a full wave p-p sensing detector, the output being fed via the load R24 to pin 2 of IC3. The loop settles at the control voltage (between 2 V and 6 V at TP14) which will provide sufficient attenuation from R15,X1 to give the correct a.f. levels at both TP8 and IC6 output. In this condition the inputs to IC3 are equal. Output amplifier IC6 has a gain of approximately x3, R6 adjusts the input off-set voltage and R7 calibrates the mod level.

93. TR7 supplies the necessary current drive for X1 (0-25 mA) and R21 thermistor compensates for the temperature coefficient of X1 attenuator. IC3 output is prevented from going negative by D5, D8 limits the differential input to IC3 when insufficient a.f. is present for the loop to level.

94. ALC limits detector, IC4 monitors the attenuator drive voltage at TP14 ensuring that it is within the limits 0-6.1 V. If the voltage is within this range D6 and D7 are unable to conduct. IC4 pin 2 is biased to approximately 0.7 V by the potential divider R29, R30, pin 3 is biased by R31, R32 to approximately 100 mV less than pin 2 causing the output of IC4 to sit at or near -12 V. As a result D10 conducts, TR1 is held off and a logic '1' +5 V (within limits) indication is passed to the microprocessor via the latches board AS2.

95. If the voltage at TP14 is less than 0 V, D7 conducts pulling IC4 pin 2 more negative thus reversing the polarity of the output. D11 conducts turning TR1 on, a logic '0' (out-of-limits) indication is passed to the microprocessor, and the a.m. or f.m. modulation OFF annunciator is repeatedly turned on and off to indicate an out-of-limits condition.

96. If the voltage at TP14 is greater than 6.1 V, D6 and D9 conduct raising the voltage at IC4 pin 3. Again the output of IC4 is reversed in polarity

causing D11 to conduct, TR1 turns on, and a logic '0' is again processed as described in the para. above.

MODULATION OSCILLATOR (AK4)

Circuit diagram : Chap. 7, Fig. 29

97. The modulation oscillator is resistor-capacitor coupled and maintained by operational amplifiers. An oscillatory loop contains a multiple feedback path filter IC3 and a drive buffer IC2. This has variable gain adjusted by a photo-coupled resistor (X1a2).

98. A diode detector D1-D5 monitors the oscillator output and drives the photo-coupler X1b2 to achieve constant output. This results in an oscillator free of amplitude variations (bounce). TR2 f.e.t. turns the oscillator off through TR1 and IC1 allowing remote control operation.

99. The oscillator has five ranges and an off position, in the off position the filter is shorted out to stop oscillation. Ranges are selected by the 5-position switch SA to give the following : (i) 400 Hz fixed, (ii) 1000 Hz fixed, (iii) 20 Hz-200 Hz variable, (iv) 200 Hz-2 kHz variable, (v) 2 kHz-20 kHz variable.

100. IC4 is the output buffer amplifier with two outputs, the first, 0 Ω, is routed via PLU pin 3 to drive the internal modulation functions. The second output 600 Ω is to the front panel socket via PLU pin 14. R18 sets the output level.

FM CONTROL (AS5)

Circuit diagram : Chap. 7, Fig. 28

101. Frequency modulation is obtained by varying the master oscillator varactor voltage on AS1. A fixed level frequency modulation signal is fed to board AS5 at PLBC pin m, also fed in on PLBC are -12 V, +12 V and +24 V d.c. supplies. A +70 V d.c. supply is supplied via PLBM pin 12.

102. A large voltage swing is required on the varactor and this is produced by a discrete low noise drive amplifier operating from the +70 V rail. The rail is highly stable and is used as a low noise reference voltage for the f.m. processing circuits.

103. In addition to f.m. the varactor provides synchronization control of the master oscillator. The synchronizer output signal 0 V-+20 V is fed to AS5 on SKBN and summed with the voltage from the front panel Fine Tune control. FM deviation control is carried out by a switched gain amplifier IC7 for coarse adjustments together with a digital-to-analogue converter IC4, IC5, IC6 for fine adjustments.

104. For wide deviations the logarithmic voltage-to-frequency characteristic of the varactor is compensated for by non-linear feedback round the varactor drive amplifier. For narrow deviations a 30 dB attenuator is switched into circuit between the varactor and its drive amplifier. The non-linear feedback is then bypassed since the varactor is essentially linear for small deviations.

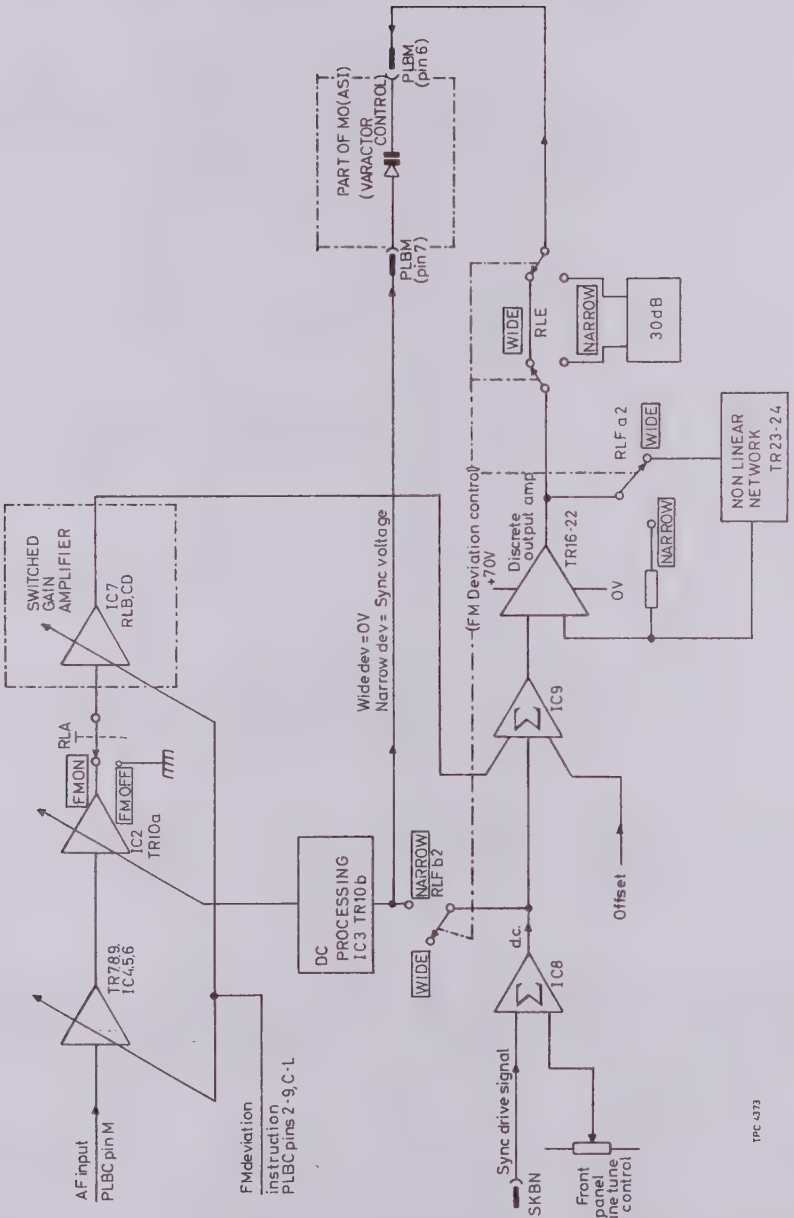


Fig. 15 FM control (AS5)

105. The synchronizer significantly changes the bias voltage on the varactor so a further gain controlled amplifier IC2 is used to maintain the calibration of narrow f.m. deviation despite changes in varactor sensitivity.

106. There are no f.m. tracking circuits since this is carried out by the microprocessor using data from a PROM. This is fixed at the time of initial calibration and requires no maintenance. Should the master oscillator require renewal a suitable programmed PROM will be supplied with it.

FM deviation (fine control)

107. A fixed f.m. signal of constant amplitude is fed to the fine control circuit from the modulation oscillator AK4 to PLBC pin M and from there to IC4 input. Fine f.m. control is achieved via PLBC with an 11-bit binary instruction from the microprocessor. The 3 m.s.b's (most significant bits) are fed from pins 6, H and 7 to a discrete D-A converter TR1 to TR9. The 8 l.s.b's (least significant bits) are fed from pins 2 to 5 and C to F to IC4, IC5, IC6 D-A converter. Outputs from both the converters are combined on the zero voltage, current summing bus connected to IC1 pin 2.

108. The output current of the lowest significant bits D-A is drawn through R61 and the most significant bits' currents are summed with this through one or more of the three resistors R38, R39 or R40 depending on which of the three f.e.t's TR7, TR8 or TR9 are switched on.

109. The 8-bit D-A converter IC4,IC5 uses two standard multiplying D-A converters, IC4 receives f.m. drive current via R56 and an offsetting current through R57 so that the input to IC4 pin 14 is always a positive current. The output of IC4 is a current whose value is proportional to the input current and the decoded 8-bit binary digital input.

110. IC5 performs the same function as IC4, R59 offsetting the input but without the audio being applied. Its digitally controlled output is fed, together with IC4 output, to IC6. This is an operational subtractor and produces an output voltage at pin 6 which is proportional to the difference between IC4 output current and IC5 output current. The offset component is common to both IC4 and IC5 and so is eliminated leaving only the digitally controlled attenuated audio voltage. This drives a current through R61 to the current summing bus.

111. TR7 switches R38 into circuit to provide the current selected by the m.s.b. of the 11 bits of the fine level data. Similarly TR8 and TR9, operated by the next two m.s.b's switch in R39 and/or R40 to add a half or a quarter respectively of the m.s.b. current to the summing bus. In the quiescent condition TR7 is normally off, driven by R32 to -12 V. A level '1' instruction turns on TR1 and TR4 causing TR7 to turn on. TR8 and TR9 are switched in an identical manner.

112. The total bus current when summed, flows through feedback resistor R22 and since IC1 pin 3 is at earth potential pin 2 will be a virtual-earth and only the output at pin 6 reflects a voltage proportional to the current of the summing bus.

113. IC2 is a variable gain amplifier and provides compensation when narrow f.m. deviations are selected, (see para. 130). The output of IC2 passes to the coarse f.m. control.

FM deviation (coarse control)

114. There are three coarse steps of f.m. deviation control, each of 10 dB, which are connected by relays to a virtual-earth operational amplifier IC7. RLA is the f.m. on/off relay; when off the relay is de-energized and the f.m. drive line is earthed. When RLA is energized (f.m. on) the drive is taken from IC2 pin 6 and through the relay on pins 7 and 4 to one or more of the relays RLB, RLC or RLD. These are energized in turn to give -10 dB, -20 dB or -30 dB steps of attenuation.

115. When all these relays are de-energized the drive is connected via the de-energized RLB and R67 to IC7 pin 2 and gives unity gain (0 dB). The three other steps are selected as shown in Table 2.

TABLE 2 FM DEVIATION COARSE CONTROL (AL4/AL5)

Relay	*State*	*Resistor coupled*	*Attenuation*
RLB	De-energized	R67	0 dB
RLB	Energized	R68	-10 dB
RLC	De-energized		
RLB	Energized		
RLC	Energized	R69	-20 dB
RLD	De-energized		
RLB	Energized		
RLC	Energized	R70	-30 dB
RLD	Energized		

Each relay is operated by a level '1' instruction turning on either TR12, TR13 or TR14 to complete the relay coil earth return. Diodes D3, D4, D5 are fitted to suppress the switch-off transient. A further 30 dB of attenuation can be switched in after the varactor drive amplifier (TR16-22) - for details of this see para. 126.

Fine tune and synchronization

116. A front panel control A0,R5 'FINE TUNE' provides 0 to +8 V d.c. and is used to alter the varactor bias voltage to fine tune the master oscillator (AS1). This voltage is added to the synchronizer control voltage fed from AL4 to AS5, IC8 via SKBN. IC8 with R71, R73, R141, R143 form an operational subtractor which eliminates earth voltage errors between the synchronizer board AL4 and AS5. Its output voltage at pin 6 is proportional to the difference between the synchronizer output voltage at SKBN (inner) and the synchronizer's earth potential on SKBN (outer). R142 provides a temporary ground when PLBN is disconnected.

117. In addition IC8 receives two offset currents, one fixed, from the +70 V rail via R139, R140, and the other variable, from the front panel 'FINE TUNE' via R145. The synchronizer output voltage range is from +2 V to +18 V with the centre voltage +10 V. (This is also the voltage fed to SKBN in the UNLOCK mode.) When the synchronizer output is +10 V and the FINE TUNE is centred, IC8 pin 6 output is at 0 V.

118. When the FINE TUNE is taken anti-clockwise i.e. wiper at +8 V, IC8 output goes positive causing a reduction in the varactor bias and when taken clockwise the reverse occurs. C30, C31 reduce the a.c. gain of IC8 to improve noise performance. D24 reduces the positive supply for IC8 to +14 V. The output of IC8 is taken via R15 to the summing amplifier IC9.

Summing amplifier IC9

119. The purpose of IC9 inverting operational amplifier is to sum the combined sync/fine tune output of IC8 and the f.m. drive from IC7 via R76 and R75 respectively. IC9 pin 3 has a fixed +6.15 V d.c. offset applied from the potential divider R78, R79. Pin 2 will also be at the same voltage due to the negative feedback path through R77. The two independent currents are then added together through R77 to give an inverted output signal at TP1. Values of R75, R76 determine the weighting factors of overall voltage gain.

Varactor drive amplifier TR16-TR22

120. This is a discrete d.c. coupled transistor amplifier with a class B push-pull output stage operating from a +70 V d.c. supply. This is obtained from PLBM pin 12. The amplifier has a high open loop gain reduced to about 2.4 by negative feedback set by R12. TR16/TR17 input comparator forces that fraction of the output voltage determined by the feedback networks to equal the input. TR20 is a high gain driver stage and TR18 is the constant current load for TR20. TR19, passing the collector current of TR18 and TR20, provides a temperature compensated bias source, with bypass C41 for the output transistors TR21 and TR22. These are complementary push-pull amplifiers. TP2, TP3, R95 provides for quiescent current monitoring of the output stage adjustable by R1. The output is taken through L1, R98 source resistor and either through a 30 dB switched pad or direct to the master oscillator via PLBM pin 6.

Non-linear feedback (wide deviation)

121. The non-linearity of the varactor diode is corrected for in the wide deviation mode by introducing non-linear feedback round the varactor drive amplifier. The linear element R12, R99 used in the narrow deviation mode is replaced by the non-linear network TR25-TR34 by the operation of RLFa2. The network changes its shunt resistance to earth as the voltage applied to it is varied.

122. The impedance variation occurs in steps of adjustable size which are arranged to closely match the varactor diodes tuning characteristic giving the combined amplifier and varactor diode a linear voltage controlled frequency law.

123. R108 to R116 provide a series of reference voltages derived from the stable low noise +70 V supply. Each reference voltage is compared with the voltage on the feedback line (RLFa2, pin 4) by a transistor-resistor-diode

network e.g. TR30, R119, R6, D16. If the feedback voltage is higher than the reference voltage, the transistor turns on, conducting current through its diode and resistors to earth. The emitter resistors R119, R6 are thus connected into the feedback circuit and conduct a current proportional to the voltage difference between the feedback rail and the voltage reference.

124. If the feedback voltage is lower than the reference voltage the transistor remains off and its emitter resistors are out of circuit. So for any voltage on the feedback line there is typically one transistor just conducting and all the lower transistors also on. All transistors above (towards TR25) are off. The total feedback network resistance is due to all the conducting stages in parallel. This resistance falls as the feedback voltage rises and turns on more of the transistors.

125. Each voltage comparator has a built-in offset voltage of two Vbe's. This is compensated for by lowering all reference voltages on the ladder by two Vbe's using TR23, D9 for the top end and TR24, D10 for the lower end. R103, R104, R105 determine the ladder reference voltages.

Wide and narrow deviation control

126. For f.m. deviations over 80 kHz (Range 8) the varactor drive amplifier output is fed directly to the varactor cathode via PLBM pin 6. However, for deviations less than 80 kHz a 600 Ω 30 dB attenuator pad comprising R18, R100, R101, R102, C51, is switched in by the relay RLE to attenuate the f.m. drive; C51 gives frequency compensation and R18 sets an exact 30 dB. The attenuator pad is not connected to earth but returned to +24 V d.c. The +24 V is supplied by IC11 pin 6 which buffers a potential divider R87, R88, R13 (+24 V adjust) connected to the +70 V d.c. low noise supply rail.

127. The quiescent output voltage of the varactor drive amplifier is also +24 V d.c. as shown in Fig. 16 below. The 30 dB pad as a result, attenuates only the applied f.m. and not the standing +24 V d.c. bias.

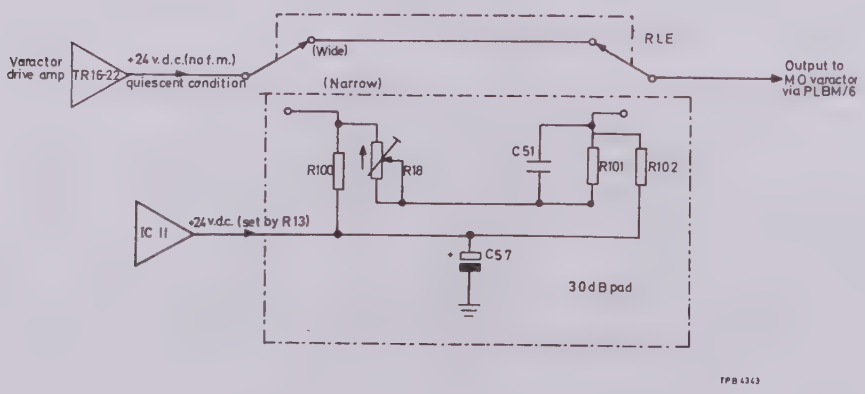


Fig. 16 Narrow deviation (30 dB) control (AS5)

128. When the 30 dB pad is in circuit RLFa2 is also energized via TR35/TR15 selecting linear f.m. drive and disconnecting the non-linear network TR23-TR34 (for details see para. 121). RLFb2 contacts switch the synchronizer drive to the varactor anode via PLBM pin 7. This prevents loss of synchronizer control caused by the insertion of the 30 dB pad which although still connected to the varactor cathode via the drive amplifier is rendered ineffective. Instead, the varactor anode receives the synchronizer drive at a similar level to the wide deviation mode and in the same phase whilst the f.m. is attenuated by 30 dB.

129. R14 sets the synchronizer control gain in the narrow mode. In the wide mode R144 provides a dummy load and the varactor anode is returned to ground via R19 and R125.

Gain compensation (narrow deviation)

130. Because the voltage-frequency characteristic of the varactor controlled oscillator is non-linear f.m. sensitivity varies with the mean varactor voltage. This has a significant effect when narrow deviations are required as the voltage normally applied to the varactor is varied over a 20 V range by the synchronizer system. To compensate for the variable sensitivity a controlled gain amplifier is included in the f.m. signal path. This is driven by the synchronizer output voltage which is available at R19 wiper and fed to IC3a, b and c to control the variable gain amplifier IC2/TR10.

131. TR10a is part of the feedback round, IC2, and operates as a voltage controlled resistor. R50, R51, R52, R53, C7 and C8 eliminate distortion to the f.m. signal. TR10b is an identical match to TR10a and operates in a d.c. mimic circuit in which IC3a/TR10b has identical gain to IC2/TR10a.

132. The junction of R41/R45 is at a potential of +8 V derived from IC10 8 V follower and the potential divider R41, R42, R43, R44 reduces this to give +4 V at IC3b pin 3, +2 V at R21 and +1 V at IC3a, pin 10. IC3b inverts, scales and offsets the synchronizer drive voltage from R19 to produce a variable reference voltage at IC3c pin 5.

133. IC3c is an integrating comparator which compares this voltage with the output of the variable gain d.c. mimic amplifier, IC3a, whose input is at +1 V (fixed). The output voltage of IC3c will settle at the value which produces the f.e.t. resistance to make the comparator inputs equal.

VCO STEERING AND MOTOR DRIVE (AS7)

Circuit diagram : Chap. 7, Fig. 33

134. Board AS7B provides the motor drive logic circuits and the clockwise and counter-clockwise motor operating relays. Board AS7A provides the following:

(1) A quiet +12 V supply for the master oscillator AS1 designed to assist the oscillator's low noise qualities and a low noise current source, the output of which is set for -0.7 V, 10 mA.

(2) A VCO (varactor controlled oscillator) steering circuit. This supplies a variable voltage derived from the master oscillator steering potentiometer AS1,R1 and gives the following outputs (a) VCO steering voltage to board AA22 to effect the Range 9, 512-1024 MHz signals and

(b) a LOW/$\overline{\text{HIGH}}$ command, initiated to change over half octave filters on board AA31 and also to change over the VCOs on board AA22, (c) a third output (0-10 V) HORIZ OUT sweep voltage also derived from AS1,R1 potentiometer is used as an external sweep voltage for XY plotters when in the Sweep mode of operation.

AS7A circuit description

135. In order to cover the frequency range of 512-1024 MHz two VCO's are used, these are situated on board AA22. Both are steered by a voltage initiated by the steering potentiometer R1, situated on the master oscillator AS1. The wiper is ganged to the main tuning controls and the voltage, determined by the position of the wiper is fed to board AS7A via PLBU pin 12 to IC1, IC3 and IC4.

136. IC3 is a comparator with a slight hysteresis built in. The output, a LOW/$\overline{\text{HIGH}}$ command is taken via PLBR pin 8 to (a) board AA31, to change over the half octave filters and (b) board AA22 (via AA21) to change over the VCO's, change over takes place when the master oscillator frequency reaches the geometric mean (355 MHz). R9 sets the voltage at the comparator, IC3, this is adjusted to be equal to the steering potentiometer wiper voltage when the master oscillator frequency is at 355 MHz.

137. The varactor diode control voltage required by each of the two range 9 VCO's on board AA22 cannot be taken directly from the steering potentiometer wiper although this is used to derive an output from IC4 as shown in Fig. 17 below.

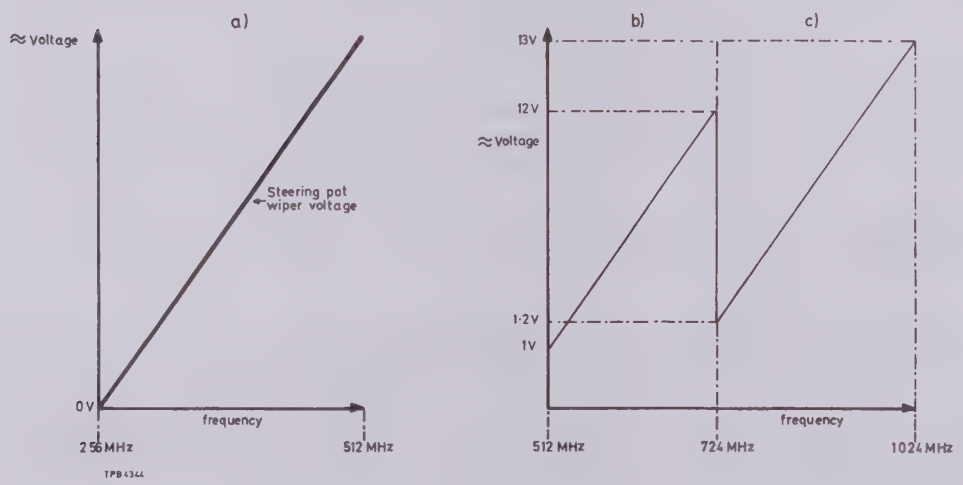


Fig. 17 Varactor diode control voltages (AS7A)

138. The steering potentiometer wiper voltage is amplified by IC4 the gain of which is controlled by the LOW/$\overline{\text{HIGH}}$ command, when LOW is asserted TR1 connects R16 in parallel with R18/R19 to give an output gain from IC4 as shown in Fig. 17(b) to control the low VCO 512-710 MHz range. When $\overline{\text{HIGH}}$ is asserted TR2 conducts connecting R17 in parallel with R18/R19 to give an output gain as shown in Fig. 17(c). R16-R19 SIC components are selected during manufacture and should not normally require further re-selection. IC4 output (VCO steering voltage) is then fed via PLBR pin J and AS6 to board AA21 PLCE pin 3.

139. IC1 also amplifies the steering potentiometer potential to give a sweep output from 0-10 V at the front panel HORIZ-OUT socket via PLBU pin 1.

AS7B circuit description

140. Motor drive. Sweep mode operation and possibly the keyboard selection of a new carrier frequency necessitates motor drive operation to change the master oscillator frequency. This is initiated by the MOTOR DRIVE $\overline{\text{ENABLE}}$ at PLBR pin B asserting low which turns TR4 and TR5 on, drawing current through R27 and R28. The potential at the junction of R27/R28 with TR6 off determines the fast drive voltage Vi (fast drive). With MOTOR DRIVE $\overline{\text{ENABLE}}$ line high, TR5 is off and Vi = 0 volts.

141. IC7 is connected to the motor in such a manner as to provide feedback control of the generated back e.m.f. Circuit values are chosen so that Vi is proportional to motor voltage less the voltage drop due to armature current, i.e. Vi is proportional to back e.m.f. and consequently controls the motor speed independent of motor loading. The fast speed is such that the main oscillator can be tuned from end to end in approximately 5 seconds.

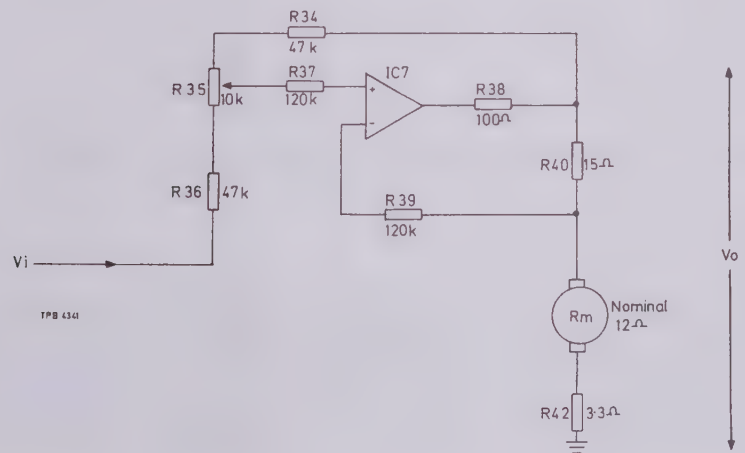


Fig. 18 Constant speed feedback circuit (AS7B)

142. As the motor drives the oscillator near to the requested frequency it is required to change to a slower drive speed in order to prevent hunting. This is approximately 1/8th of the fast speed and is achieved when MOTOR $\overline{\text{FAST DRIVE}}$ signal at PLBR pin E goes high turning TR6 on. As a result R29 is connected in parallel with R28 to give a reduced Vi (slow drive) - see Fig. 19(b).

143. In the SWEEP mode, SWEEP $\overline{\text{ON}}$ signal at PLBR pin 7 is asserted low, TR6 is turned off and TR7 on. This connects a potentiometer chain consisting of R31, R30 and the variable front panel SWEEP RATE control AOR2 so that Vi (sweep) is a variable proportion of Vi (fast drive), see Fig. 19(c).

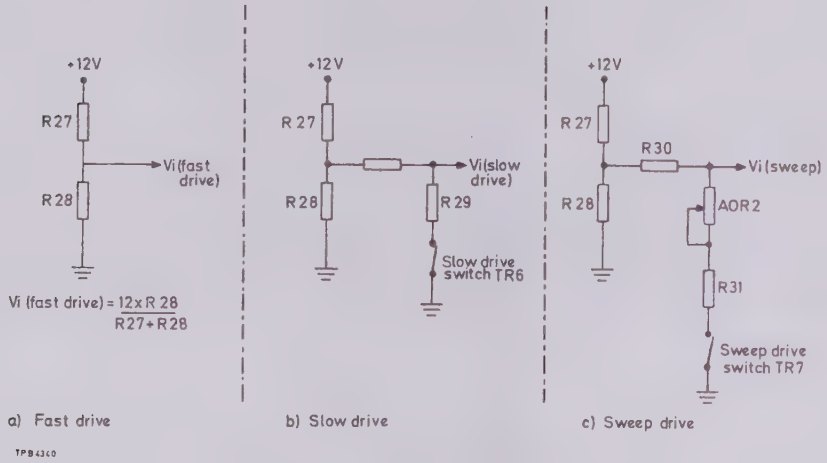


Fig. 19 Fast, slow and sweep motor drive control (AS7B)

Motor direction

144. Power is applied to the motor via PLBR pins 1 and 2 when either Relay A (clockwise) or Relay B (counter-clockwise) is energized. When the MOTOR CW/$\overline{\text{CCW}}$ line at PLBR pin H is high and MOTOR $\overline{\text{ENABLE}}$ line goes low, TR8 turns on and Relay A is energized. When MOTOR CW/$\overline{\text{CCW}}$ line is low and MOTOR $\overline{\text{ENABLE}}$ line goes low, TR9 turns on and Relay B is energized. When MOTOR $\overline{\text{ENABLE}}$ line is high the motor is short circuited and stops immediately preventing carrier frequency overshoot.

145. A protection device has been incorporated in the motor gearbox. If the motor exceeds its allowable clockwise rotation limit a micro-switch operates forcing MOTOR $\overline{\text{CW END}}$ line low opening Relay A. This prevents further clockwise travel. A similar micro-switch prevents the motor from exceeding its allowable counter-clockwise rotation limit by forcing MOTOR $\overline{\text{CCW END}}$ line low and opening Relay B.

146. Current protection. The motor is protected against accidental burn out by current limiting to 200 mA, this is carried out by the action of R42 and TR11.

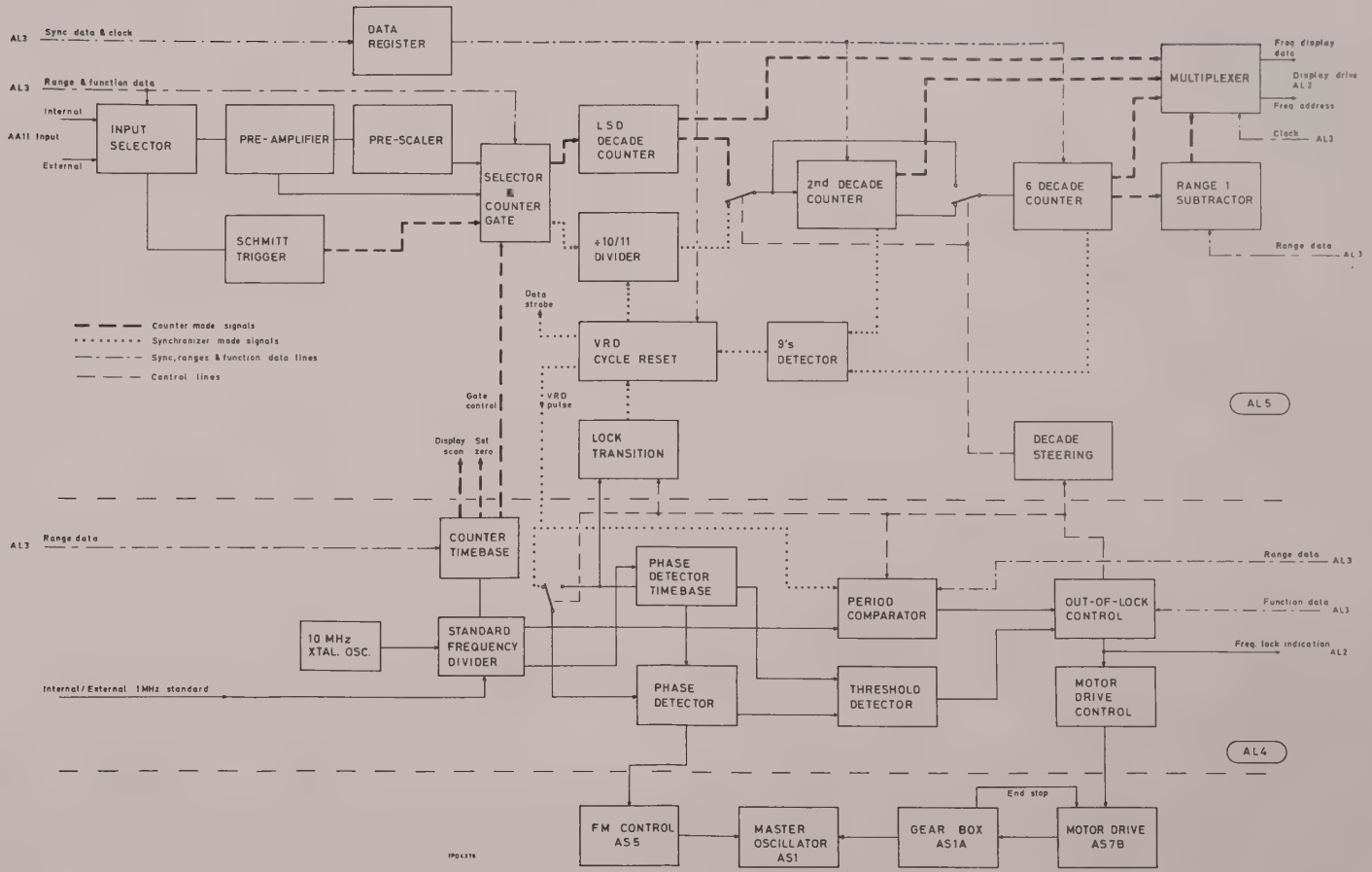


Fig. 20 Counter/synchronizer simplified block diagram (AL4/AL5)

SYNCHRONIZER/COUNTER 'A' (AL5) - see Fig. 20

Circuit diagram : Chap. 7, Fig. 12

147. Synchronizer/counter 'A' board AL5 operates in conjunction with synchronizer/counter 'B' board AL4 to provide two main functions:-

(1) In the Frequency Lock mode AL4 and AL5 provide frequency synchronization. Electrical (fine) tuning is derived from the variable ratio divider (VRD) together with phase detector, and motor (coarse) tuning is derived from a frequency (or period) comparator.

(2) In the Manual or Unlocked Frequency mode the VRD circuit is reconfigured as a standard decade counter providing the frequency display data (motor tuning is disabled).

(3) A subsidiary function enables AL4 and AL5 to act as a counter to externally applied signals.

Counter mode - see Fig. 21

148. The Counter mode of operation gives continuous monitoring of the carrier frequency in the Manual (UNLOCK) mode. It provides for a 7½ decade display of carrier frequencies from 10 kHz to 1024 MHz with a resolution of 10 Hz below 128 MHz, and 100 Hz above 128 MHz. The counting process in AL5 varies according to the selected range as shown in Table 3.

TABLE 3 COUNTING PROCESS (AL4/AL5)

Generator range	*Generator carrier freq.*	*AL5 input signal freq. (SKAB)*	*Counter circuit freq. (TP14)*	*Display resolution*
1	10kHz-4MHz	4.01-8MHz	4.01-8MHz	10Hz
2-6	4-128MHz	4-128MHz	4-128MHz	10Hz
7,8	128-512MHz	128-512MHz	32-128MHz	100Hz
9	512-1024MHz	256-512MHz	64-128MHz	100Hz

It should be noted that AL4 input signal frequency is offset by 4 MHz from the carrier frequency on range 1 and is half the carrier frequency on range 9. Additionally the counter may be used to count external frequencies from 10 Hz to 500 MHz in any one of three ranges :

(a) 10 Hz to 10 MHz, resolution 1 Hz.

(b) 1 MHz to 100 MHz, resolution 10 Hz.

(c) 10 MHz to 500 MHz, resolution 100 Hz.

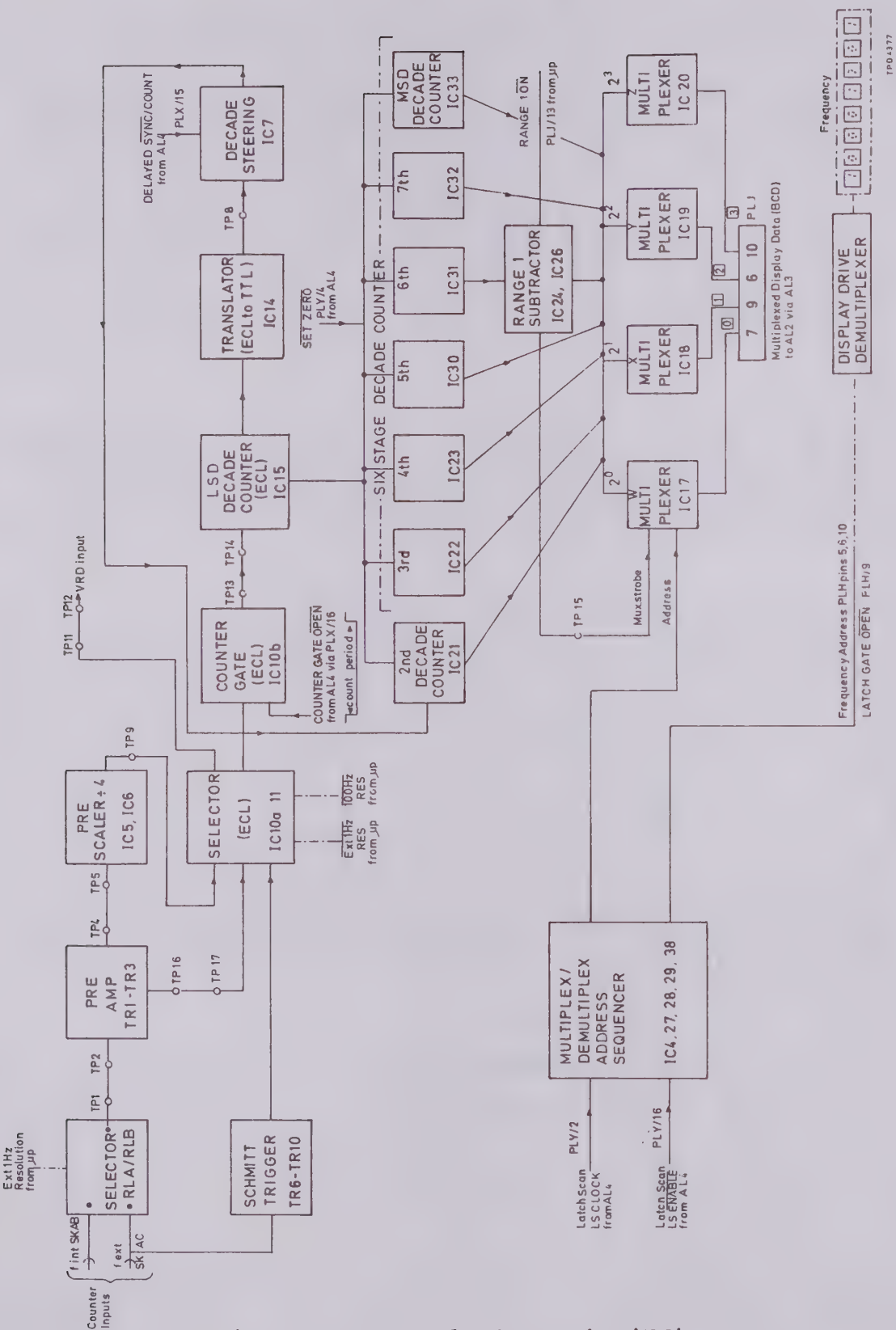


Fig. 21 Counter mode of operation (AL5)

149. The following sub-units are used in the counting processes.

Pre-amplifier. Circuit TR1-TR3 provides amplification and shaping of signals between 1-500 MHz, output at TP16 has emitter coupled logic (ECL) compatible amplitude.

Pre-scaler. High speed dividers IC5,IC6 give a frequency division by a factor of 4 to limit the maximum counter frequency to 130 MHz, output at TP9 is ECL compatible.

Schmitt trigger. Circuit TR6-TR10 shapes the 10 Hz-10 MHz external signal waveform. Input sine waves of sufficient amplitude (greater than 100 mV) are shaped to give a square wave output at TP10 with a fast transition time and ECL compatible level.

Selector and counter gate. IC10 and IC11 are ECL NOR gates providing operation up to 130 MHz and select the appropriate input from pre-amplifier TP17, pre-scaler TP9 or Schmitt trigger TP10. A non-gated output at TP11 provides the input signal to the variable ratio divider (VRD). A gated output at TP13 provides the gated signal input to the counter circuit. The gate period is that time which the COUNTER GATE $\overline{\text{OPEN}}$ 'low' instruction (PLX pin 16) is asserted.

Counter. This is an 8 decade asynchronous counter fed from a gated signal input at TP14. The first decade counter, IC15, is an ECL device providing division by 10 with 130 MHz capability. IC14 translates IC15 output from ECL to TTL levels. Subsequent decade counters IC21-IC23 and IC30-IC33 are TTL devices. The decade outputs are multiplexed and update the display during each gate reset period.

Range 1. Here the counter output is decremented by 4 MHz to display 10 kHz-4 MHz from the 4.01-8 MHz input. An error indication (-1) occurs if the carrier frequency control is tuned below zero beat.

Counter input signal routeing (AL4/AL5)

150. Routeing of signals in the following modes of operation are governed by microprocessor instruction and front panel control settings. Conditions for each operating mode are shown in Table 4 below.

TABLE 4 COUNTER/VRD INPUT SIGNAL ROUTEING (AL4/AL5)

Operating mode	*Freq. range*	*Display resolution*	*Function control lines*				*Countergate period*
			Sync/ count	*Ext 1Hz res*	*Ext 1Hz res*	*100Hz*	
UNLOCK	(0.01-128MHz) 1-6	10Hz	High	High	High	High	100ms
UNLOCK	(128-512MHz) 7,8	100Hz	High	High	High	Low	40ms
UNLOCK	(512-1024MHz) 9	100Hz	High	High	High	Low	80ms
* LOCK	(0.01-128MHz) 1-6	10Hz	Low	High	High	High	-
* LOCK	(128-1024 MHz) 7-9	100Hz	Low	High	High	Low	-
EXT	10Hz-10MHz	1Hz	High	High	Low	High	1s
EXT	1-100MHz	10Hz	High	Low	High	High	100ms
EXT	10-500MHz	100Hz	High	Low	High	Low	40ms

* VRD function

There are eight sets of conditions described as follows:-

151. Unlock mode, ranges 1-6 (0.01-128 MHz). Here the signal is routed from the input socket , SKAB, through relay RLA, pre-amplifier, and selector gate IC10 to counter input TP14.

152. Unlock mode, ranges 7, 8 (128-512 MHz). To maintain signal frequencies within counter operating range, signals above 128 MHz are routed from SKAB through RLA, pre-amplifier and pre-scaler. The pre-scaler output is gated by ECL selector IC10 and fed to the counter input TP14.

153. Unlock mode, range 9 (512-1024 MHz). In this mode the function lines operated are identical to range 7 and 8. The only difference being that the gate period is extended from 40 ms to 80 ms.

154. Lock mode, ranges 1-6. The signal is routed from the input socket SKAB, through relay RLA, pre-amplifier circuit, and selector IC10a, IC11b to the VRD input TP12. Counter gate operation is inhibited in the Lock mode (PLX pin 16 is high).

155. Lock mode, ranges 7-9. The signal is routed from the input socket SKAB, through relay RLA, pre-amplifier, pre-scaler, and selector IC10a, IC11b to VRD input TP12. Counter gate operation is inhibited (PLX pin 16 is high).

156. External counter input (10 Hz-10 MHz). Signals in the range 10 Hz to 10 MHz are fed from the front panel socket via SKAC direct to the Schmitt trigger circuit. Input is high impedance with relay RLB de-energized. Output at TP10 is routed via selector gate IC11a, IC10b to the counter input TP14.

157. External counter input (1-100 MHz). Input for this range is via SKAC, through RLB, energized by the EXT 1 Hz RES control line. Signals are then routed through the pre-amplifier and selector gate IC10 to the counter input TP14.

158. External counter input (10-500 MHz). Here the input is via relay RLB, control lines $\overline{\text{EXT}}$ $\overline{\text{1 Hz}}$ $\overline{\text{RES}}$ and $\overline{\text{100 Hz}}$ are asserted to route the signal through both pre-amplifier, pre-scaler, and selector gate IC10 to the counter input TP14.

Decade counter operation (Unlock mode) (AL4/AL5)

159. There are seven counter operating modes that require a front panel indication of frequency, these are shown in Table 5 below. Input signals are routed from SKAB or SKAC to counter input TP14 as described previously. Counter gating periods are controlled by the COUNTER GATE $\overline{\text{OPEN}}$ control line, the periods of which are also shown in Table 5 below. On completion of counter gate period the content of the counter is multiplexed and fed to the front panel frequency display. The $\overline{\text{SET ZERO}}$ control line resets all decades to zero prior to the counter gate re-opening.

TABLE 5 COUNTER MODES OF OPERATION (AL4/AL5)

Operating mode	*Range*	*Display resolution*	*Counter gate period*	*Range 1 $\overline{on}$*
UNLOCK	1	10 Hz	100 ms	Low
UNLOCK	2-6	10 Hz	100 ms	High
UNLOCK	7-8	100 Hz	40 ms	High
UNLOCK	9	100 Hz	80 ms	High
EXT	10Hz-10MHz	1 Hz	1 s	High
EXT	1MHz-100MHz	10 Hz	100 ms	High
EXT	10MHz-500MHz	100 Hz	40 ms	High

160. Multiplexer operation. BCD outputs from the decade counters are fed to four data selector multiplexers IC17-IC20. The parallel b.c.d. data is fed out sequentially when the 3-bit frequency address cycles from 0, through 1 to 7 and back to 0. This sequential data is fed to AL2 via PLJ pins 6, 7, 9, 10 where it is de-multiplexed and fed to 8 digits of display on board AL1 to provide the frequency display - see Fig. 22.

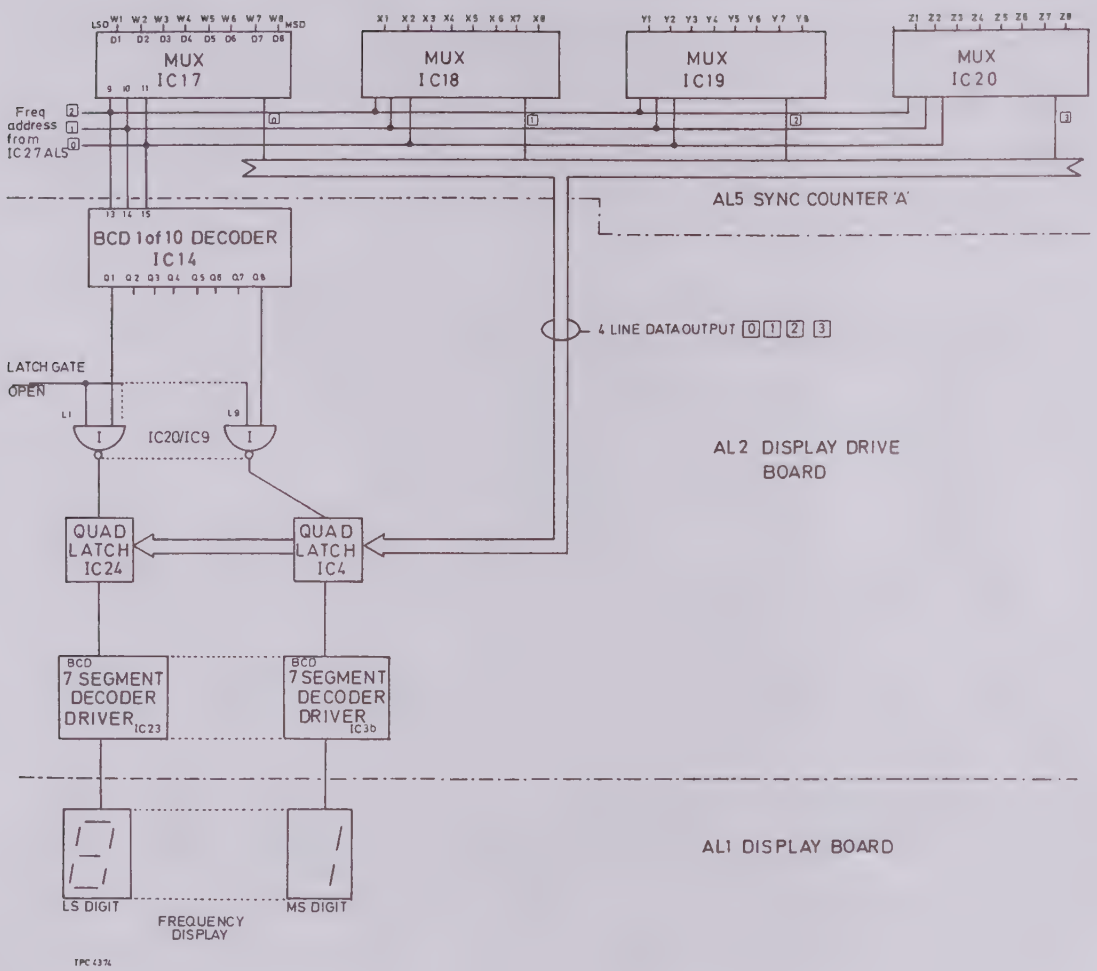


Fig. 22 MUX/Decoder 8 digit display; Counter mode (AL1,AL2,AL5)

MUX/DEMUX address sequencer

161. The circuit providing the 3-bit frequency multiplexer address is shown in Fig. 24. The address cycle is generated whenever LS $\overline{\text{ENABLE}}$ goes 'low', this occurs during every counter gate reset period. Waveforms appropriate to the circuit are shown in Fig. 23.

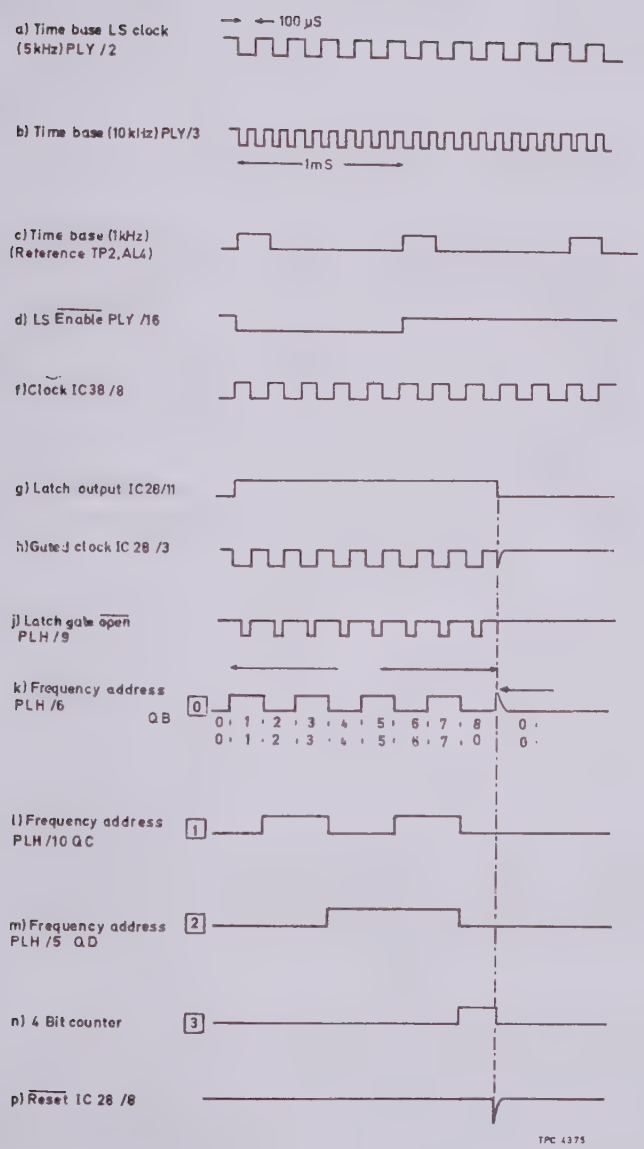


Fig. 23 MUX/DEMUX Counter mode timing waveforms (AL5)

162. In the counter mode LS $\overline{\text{ENABLE}}$ going low sets the latch IC28, thereby enabling the CLOCK GATE. LS CLOCK signals at 5 kHz cause 4-bit counter IC27 to count from 0 to 1 and then through to 8. The 9th clock pulse is detected and generates a $\overline{\text{RESET}}$ pulse of transient duration since it resets the 4-bit counter to zero; it also resets the latch so that the CLOCK GATE now inhibits further LS CLOCK signals. Circuit will remain in this state until the next LS $\overline{\text{ENABLE}}$ pulse.

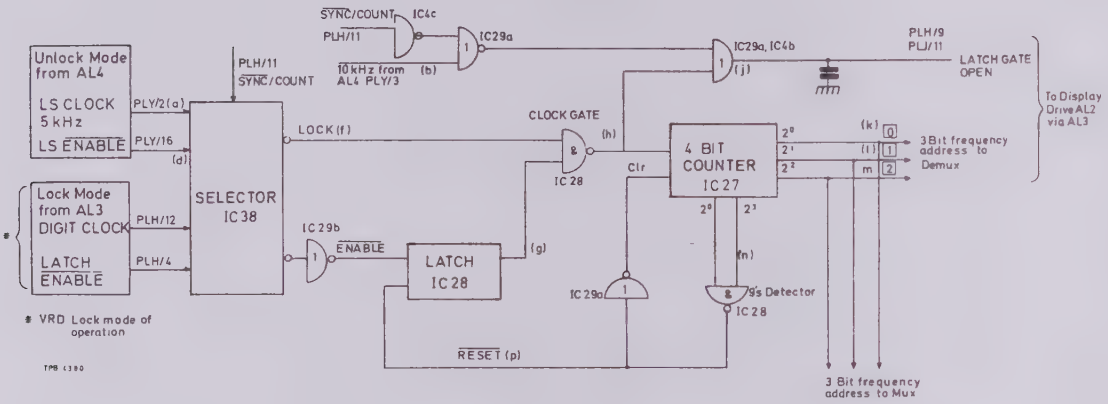


Fig. 24 MUX/DEMUX address sequencer (AL5)

163. The gated clock signal is further gated in IC29a/IC4b with 10 kHz to provide 8 pulses on the LATCH GATE $\overline{\text{OPEN}}$ line. These enable the de-multiplexer quad data latches on AL2 during periods when the data is stable, i.e. avoids the transitions of de-multiplexer address.

Range 1 (10 kHz-4 MHz) subtractor - see Fig. 25

164. On ranges 2-9 the display frequency is identical to the count frequency. Table 3 shows that on range 1, AL5 input frequency at SKAB of 4.01-8 MHz corresponds to a carrier frequency of 10 kHz-4 MHz, therefore the display must read 10 kHz-4 MHz. This is achieved by the range 1 subtractor circuit IC24, IC26, which effectively subtracts 4 MHz from the count. On selecting range 1, PLJ pin 13 RANGE 1 $\overline{\text{ON}}$ is asserted causing the subtractor outputs to change to those shown in Table 6 (b) below.

TABLE 6 RANGE 1 RECODING (AL5)

(a)

	Decade 6 display		*IC31 COUNT* 0	1	2	3	4	5	6	7	8	9	
Ranges 2-9 Range 1 $\overline{ON}$ 'high'	W6	QA	0	1	0	1	0	1	0	1	0	1	1
	X6	QB	0	0	1	1	0	0	1	1	0	0	2
	Y6	QC	0	0	0	0	1	1	1	1	0	0	4
	Z6	QD	0	0	0	0	0	0	0	0	1	1	8
													BCD

(b)

	Decade 6 display		*Amended Range 1 display* 0	1	2	3	0	1	2	3	4	5	
Range 1 Range 1 $\overline{ON}$ 'low'	W6	QA	0	1	0	1	0	1	0	1	0	1	1
	X6	QB	0	0	1	1	0	0	1	1	0	0	2
	Y6	QD	0	0	0	0	0	0	0	0	1	1	4
	Z6	0	0	0	0	0	0	0	0	0	0	0	8
													BCD

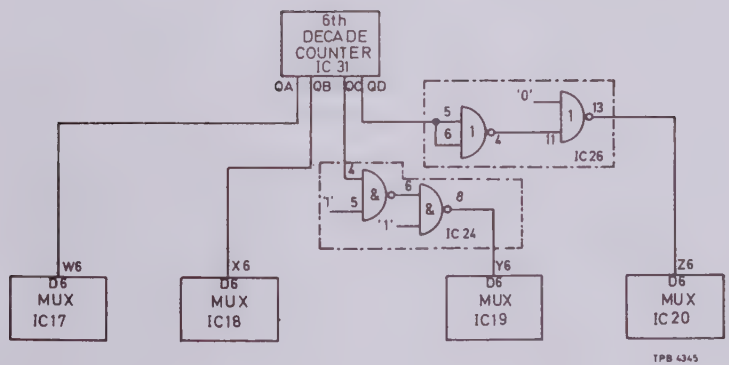


Fig. 25 Ranges 2-9 decade counting (AL5)

165. Recoding of the logic QC and QD count of the sixth decade counter is carried out as shown by the simplified logic diagram shown below in Fig. 26.

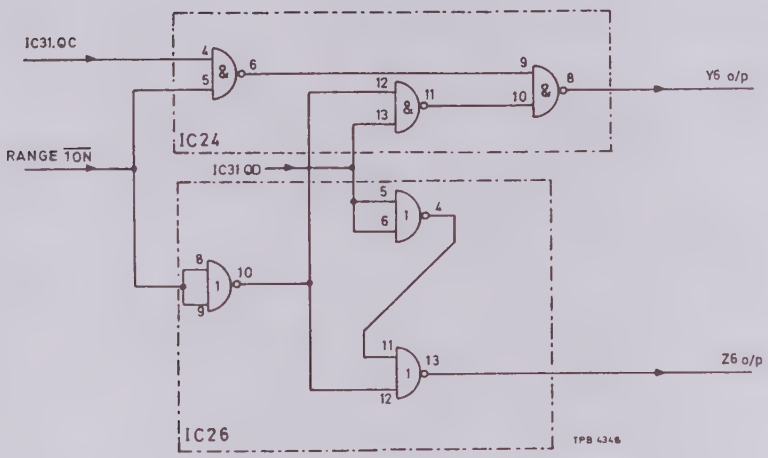


Fig. 26 Range 1 subtractor circuit (AL5)

Range 1 blanking (under-ranging) - see Fig. 27

166. Manual tuning on range 1 is achieved by additive mixing of the variable 4.01-8 MHz signal with a fixed 4 MHz frequency. If the variable signal is reduced below 4 MHz, erroneous carrier signals are produced. This state is indicated by a frequency error display of -1. With RANGE 1 $\overline{ON}$ 'low' MUX strobe, TP15, is held high whenever the sixth decade counter output is less than 4, i.e. QC and QD both 'low'. With the MUX strobe thus disabled the data fed to each display digit is binary 1111 resulting in a blanked display except for the m.s.d. which indicates -1.

167. The display of an invalid count is inhibited on all ranges following transition from the LOCK mode of operation to the UNLOCK mode. In the locked mode the latch output is held low disabling the MUX strobe. Switching to the UNLOCK mode gives an initial error display of -1 before the first $\overline{SET\ ZERO}$ pulse resets the latch thereby enabling the MUX strobe for subsequent counts.

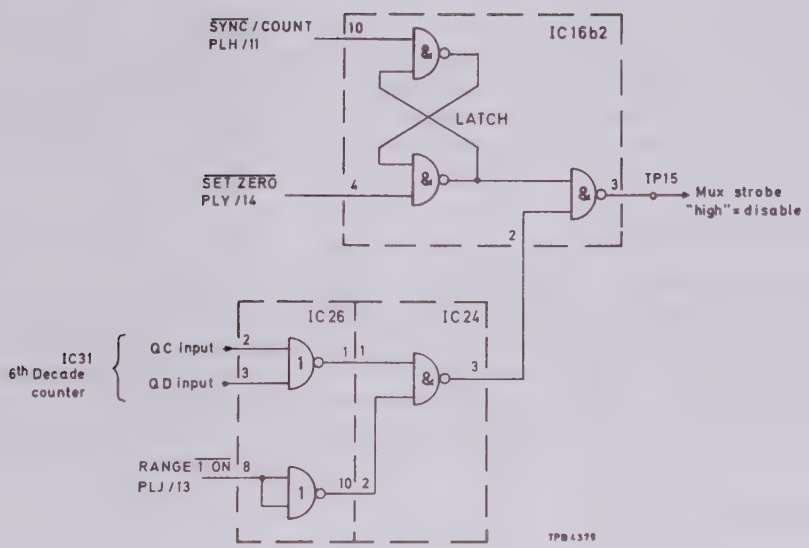


Fig. 27 Range 1 under-ranging circuit (AL5)

Frequency lock mode (synchronizer operation)

168. RF input to the synchronizer circuit is routed through the input selector circuit as described previously in AL5 Counter mode of operation. The signal frequency is divided in the variable ratio divider (VRD) by a ratio set by the microprocessor. The output of the VRD is a pulse (the VRD pulse) whose repetition rate is compared with the frequency standard in a phase detector (part of AL4). The output of the phase detector provides the fine tuning voltage for the master oscillator, the overall feedback stabilizing the oscillator frequency. A frequency error of ±500 p.p.m. is corrected to ±1 p.p.m. in 3.5 s. Coarse tuning is derived from a period comparator (part of AL4) whose output controls the tuning motor drive. Frequency display is derived from instructions received via the microprocessor.

Variable ratio divider - see Fig. 28

169. The variable ratio divider consists of a programmable dual modulus divider followed by seven pre-settable decade counters together with cycle reset circuitry. The division ratio is determined by the sync data loaded into the dual modulus controller and decade counters.

Dual modulus divider

170. To provide the pre-set decade counters with a frequency within their range (maximum 50 MHz) the input frequency is divided down in a u.h.f. programmable divider with ÷10 or ÷11 division ratios. This divider is basically an ECL device with 200 MHz input capability and TTL compatible output. Overall counter speed is limited by its reset time and with the pre-settable

counters used, a reset pulse width of 30 ns is required. The counter is designed to accommodate this reset delay without producing errors at high clock rates. IC1 can be instructed to divide by 10 or 11 at any time up to half way through its count cycle, so allowing a reset time of approximately five times that of the input clock period to be used.

Pre-set decade counters

171. The decade counters operate as 9's complement ratio dividers controlled by sync data from the microprocessor. At the start of each division cycle IC1 divides by 11 B0 times, where B0 is the least significant digit (l.s.d.). After the B0 divisions the l.s.d. decade counter (IC13) registers 9, this state is detected by 9's detector (IC9) whose output resets ÷10/11 latch IC9. This in turn instructs IC1 to now divide by 10, and IC13 to stop counting.

VRD cycle reset

172. Decade counters IC21-23, IC30-33 continue the count until the 9's detectors IC12, IC25/26 are activated and operate the cycle reset latch IC3. This provides the VRD PULSE which is fed to AL4, and also the DATA STROBE pulse which initiates the start of the division cycle by loading 9's complement data into each decade counter. It also resets the ÷10/11 latch so that IC1 again divides by 11.

Principle of VRD operation

173. The function of the VRD is to produce a pulse output with a fixed p.r.f. (see Table 7) whenever the carrier frequency corresponds to the VRD division ratio as determined by the microprocessor sync data. In this state the frequency is said to be locked. The general expression for the division ratio, R of such a VRD is

$$R = 11(B0) + 10(B1 + 10B2 + 10^2B3 + 10^3B4 + 10^4B5 + 10^5B6 + 10^6B7 - B0)$$

where B0, B1, B2 --- B7 etc. represent the digits of the division ratio l.s.d. (B0) through to m.s.d. (B7).

TABLE 7 FREQUENCY DIVISION IN THE VARIABLE RATIO DIVIDER (AL5)

Range	*Resolution (Hz)*	*Carrier Frequency (MHz)*	*AL5 Input Frequency (MHz)*	*VRD Input Frequency (MHz)*	*VRD Division ratio*	*VRD pulse p.r.f. (Hz)*
1	10	.01-4	4.01-8	4.01-8	401000-800000	10
2-6	10	4-128	4-128	4-128	400000-12800000	10
7,8	100	128-512	128-512	32-128	1280000-5120000	25
9	100	512-1024	256-512	64-128	5120000-10240000	12.5

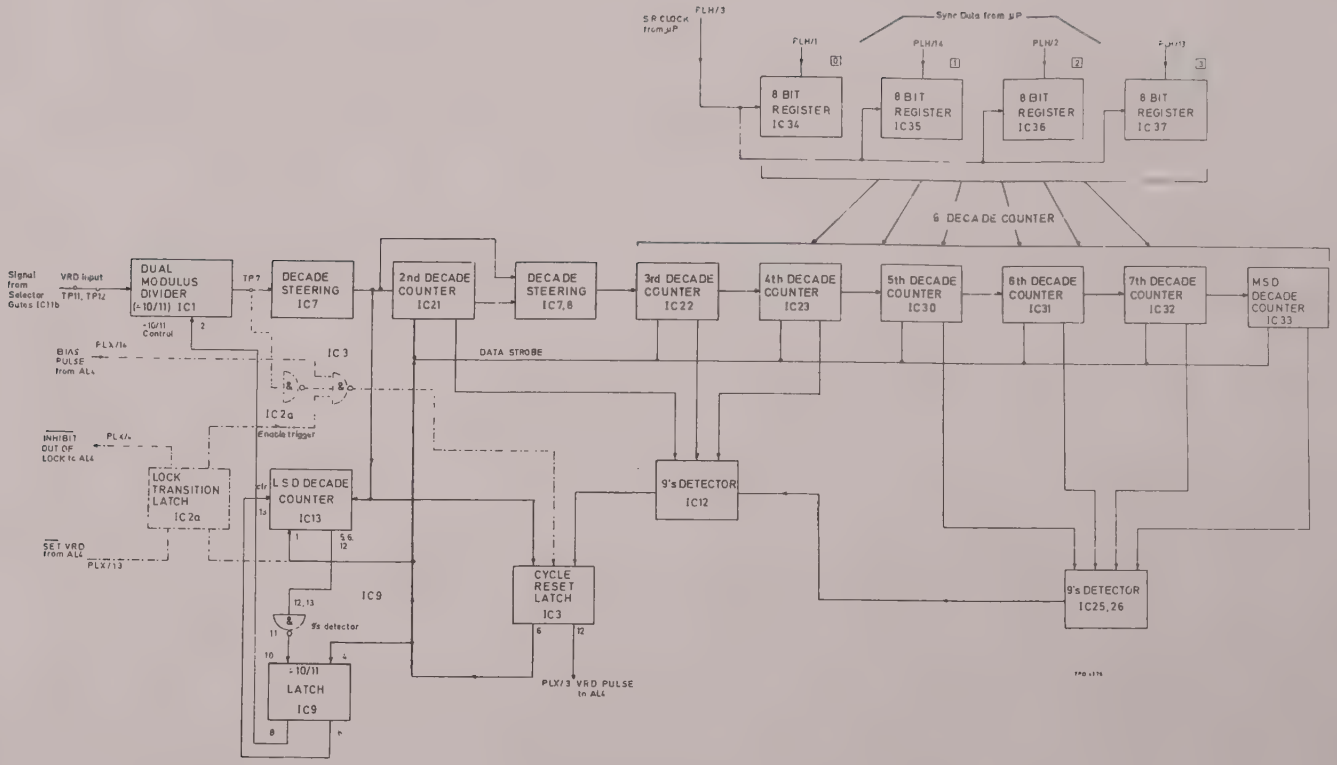


Fig. 28 Variable ratio divider in Frequency Lock mode (AL5)

174. If, for example, the required carrier frequency is 12.34567 MHz (range 3, 10 Hz resolution) then

$$B0 = 7,\ B1 = 6,\ B2 = 5,\ B3 = 4,\ B4 = 3,\ B5 = 2,\ B6 = 1,\ B7 = 0$$

$$\therefore \text{ Division ratio } R = 11x7+10\ (6+10x5+100x4+1000x3+10000x2+100000x1-7)$$

$$= 77+10\ (123449) = 1234567$$

Hence 12.34567 MHz is divided down to give a VRD pulse output of p.r.f. 10 Hz, i.e. pulses at 100 ms intervals. A shift of input frequency from that set by the VRD causes the interval between output pulses to change; this results in the appropriate correction to the oscillator fine tune voltage.

175. The VRD circuit operates in the 9's complement mode, so that instead of counting from 0 to R ≡ B7, B6, B5, B4, B3, B2, B1, B0, the same division ratio is achieved by counting from A7, A6, A5, A4, A3, A2, A1, A0 to 99999999 where A is the 9's complement of B i.e. A0 = 9-B0, A1 = 9-B1, etc. The sync data from the microprocessor consists of 9's complement data A7 - A0 corresponding to the division ratio B7 - B0. In the above example A7 = 9-0=9, A6 = 9-1=8, A5 = 9-2=7, A4 = 9-3=6, A3 = 9-4=5, A2 = 9-5=4, A1 = 9-6=3, A0 = 9-7=2 so that the count cycle is initiated with counter content = 98765432.

176. The action of counting by the two lowest counters is shown below.

		IC13	*IC21*
(1)	Initial sync data from microprocessor	A0=2	A1=3
(2)	After 11 input pulses to dual modulus divider	2 advances to 3	3 advances to 4
(3)	" 22 " " " " " "	3 " " 4	4 " " 5
(4)	" 33 " " " " " "	4 " " 5	5 " " 6
(5)	" 44 " " " " " "	5 " " 6	6 " " 7
(6)	" 55 " " " " " "	6 " " 7	7 " " 8
(7)	" 66 " " " " " "	7 " " 8	8 " " 9
(8)	" 77 " " " " " "	8 " " 9 (full)	9 " " 0+ carry

At this point the 1.s.d. decade counter is full and initiates a reset pulse to the ÷10/11 latch so that IC1 subsequently divides by 10 so that the counter is now 9876550(9). The carry advances IC22 from A2=4 to 5.

177.

	IC13	*IC21*
(9) After 157 input pulses Counter content is now 9876558(9).	9 (full)	7 advances to 8

(10) After each subsequent 100 pulses IC22 advances by 1 so that after 557 input pulses counter content is 9876598(9). Similarly IC23 initially set at A3=5 advances by 1 after each further 1000 pulses, so that after 4557 input pulses the counter content is 9876998(9). In this way after 1234557 input pulses, counter content is 9999998(9) and 9's detector IC12, IC25/26 initiates the reset cycle in latch IC3. During the next 10 input pulses the VRD PULSE and DATA STROBE pulse are generated, so that after 1234567 input pulses the reset cycle is complete and the count cycle starts again.

Out-of-lock state (AL4/AL5)

178. The VRD output is monitored by a period comparator in AL4 which controls the coarse tuning (motor drive). In the out-of-lock state a fast data rate is required to give precise motor control. This is achieved by the decade steering bypassing the 2nd decade counter IC21 when DELAYED $\overline{\text{OUT OF LOCK}}$ command, PLX pin 2, is asserted low. VRD p.r.f's in this condition are as follows:-

Ranges 1-6 : 100 Hz

Ranges 7-8 : 250 Hz

Range 9 : 125 Hz.

Lock transition circuit (AL4/AL5) - see Fig. 29

179. The function of this circuit is to enable the locked mode of operation to be entered without carrier frequency perturbation. This gives a smooth frequency transition in going from Unlocked (manual) to Locked mode of operation. The circuit also minimizes frequency settling time following a period of coarse (motor) tuning. To achieve the desired result it is necessary for the oscillator fine control voltage in the Locked mode to be initially the same as in the Unlocked mode.

180. The oscillator fine control voltage is derived from the phase detector in AL4 board, by sampling a ramp voltage whose repetition rate, 100 Hz, is tied to the frequency standard. In the Unlocked mode, or out-of-lock state, sampling occurs at the centre of each ramp giving a fixed fine control voltage. In the Locked mode sampling occurs coincident with each VRD PULSE on every 10th ramp on ranges 1-6, every 4th ramp on ranges 7, 8 and every 8th ramp on range 9. Smooth frequency transition can be achieved by constraining the first VRD PULSE to be in phase with the centre of the ramp.

181. In the transition circuit the BIAS PULSE is used to sample at the centre of the phase detector ramp (AL4) in the Unlocked mode and out-of-lock state. When the lock state is entered a $\overline{\text{SET}}$ VRD pulse is generated which sets the lock transition latch. This inhibits the VRD 9's detector and partly enables the trigger gate IC3 which is fully enabled when the BIAS PULSE arrives. The consequent negative trigger at TP6 sets the VRD cycle reset latch generating the first VRD PULSE and DATA STROBE which initiates the first VRD cycle. The lock transition latch is reset so that the VRD circuit subsequently operates normally, transition waveforms are illustrated in Fig. 33.

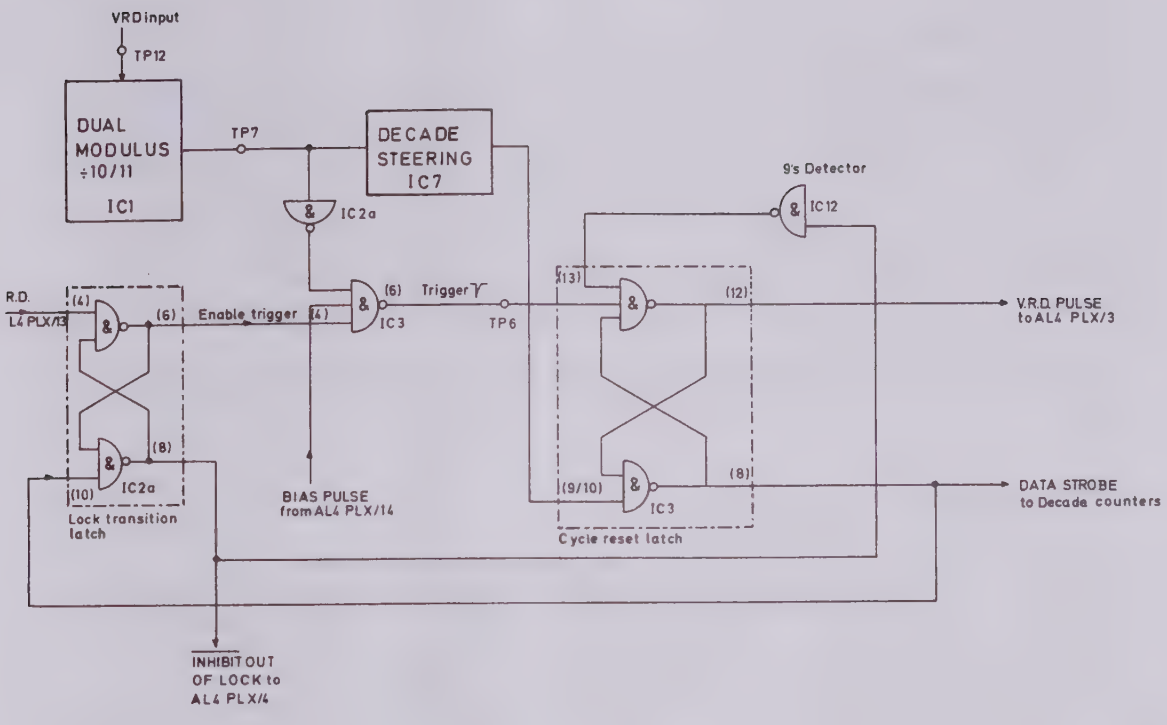


Fig. 29 Lock transition circuit (AL5)

SYNCHRONIZER/COUNTER 'B' (AL4) - see Fig. 20

Circuit diagram : Chap. 7, Fig. 11

182. Synchronizer/counter 'B' board AL4 operates in conjunction with synchronizer/counter 'A' board AL5 to provide three main functions :

(i) Counter time base. Time base waveforms are derived from the frequency standard and drive the counter circuit in AL5.

(ii) Motor drive (coarse frequency) control. In the Synchronizer mode of operation the output of the variable ratio divider (VRD) in AL5 is monitored by a period comparator. Variations in the VRD period activate the motor drive circuit.

(iii) Phase detector (fine frequency) control. In the Synchronizer mode of operation the phase of the VRD pulse is converted to an electrical fine tuning voltage in the phase detector. This provides the feedback necessary to stabilize the oscillator frequency in the locked state.

Standard dividers - see Fig. 30

183. The accuracy of the counter and locked frequency is directly related to the frequency standard via the standard divider chain. Internal frequency standard is maintained by a temperature stabilized 10 MHz crystal oscillator, X1. After division by 10 in IC1a, a buffered 1 MHz standard is available at SKDP on the rear panel. An external 1 MHz standard (4 V p-p t.t.l. or 1 V r.m.s. sine wave) may be connected to socket SKDP in place of the internal frequency standard. Selection is made by the rear panel EXT STD IN switch. When this is used the internal crystal oscillator is disabled to prevent a low frequency beat note between two standard frequencies causing spurious f.m.

184. The 1 MHz standard is further divided down in IC1b and IC6 to provide a 1 kHz counter time base clock at TP2, and a 1 kHz VRD time base clock at IC6 pin 10.

Counter time base - see Fig. 30

185. The circuit provides the waveforms to drive the counter in AL5. The counter gate period is directly related to the frequency standard by further sub-division of the 1 kHz waveform at TP2 providing the COUNTER GATE $\overline{\text{OPEN}}$ control line at PLX pin 8. The reset cycle between counter gate periods is a fixed 4 ms during which an LS $\overline{\text{ENABLE}}$ pulse is generated at PLY pin 8, enabling AL5 counter contents to be multiplexed, and a $\overline{\text{SET}}$ ZERO pulse at PLY pin 6 resets AL5 counter to zero. Range data from the microprocessor controls the counter gate periods, details of these are given in Table 4.

186. The counter time base circuit is shown in Fig. 30. The appropriate counter gate period, Nms, is derived from the 1 kHz standard at TP2 by division by 2N. This is determined by the time base selectors IC12/PLY pin 1, IC24/PLY pin 16, and IC25/PLY pin 13, e.g. 100 ms counter gate period is derived by a division of 200 made up of ÷10 in IC17a, ÷2 in IC23 and ÷10 in IC17b.

187. The operation of the time base reset is shown in the simplified diagram Fig. 30b. During the count period COUNTER GATE $\overline{\text{OPEN}}$ is 'low' and GATE RESET $\overline{\text{ENABLE}}$ is 'high' holding the gate reset counter at zero. At the completion of the count period GATE RESET $\overline{\text{ENABLE}}$ goes 'low' enabling the gate reset counter to advance every ms. After 4 ms GATE PERIOD RESET goes 'high' resetting the gate period counter to its initial zero state, COUNTER GATE $\overline{\text{OPEN}}$ goes low and the cycle recommences. The gate reset counter output is decoded to give LS $\overline{\text{ENABLE}}$ pulse when reset count is 1, and SET $\overline{\text{ZERO}}$ pulse when the reset count is 3.

188. In the Synchronizer mode of operation the time base circuit is used to provide a 6.25 Hz square wave to control the frequency lock indicator flashing rate. The hold line being high inhibits the GATE PERIOD RESET so that the time base dividers free run; since the division ratio between TP2 and TP8 is 160, TP8 output is a 6.25 Hz square wave.

Period comparator - see Fig. 31

189. In the Synchronizer mode of operation the variable ratio divider (VRD) in AL5 produces a VRD PULSE output whose period is a function of the signal frequency and the programmed division ratio. When the frequency is locked the VRD period is an exact multiple of 10 ms as follows:

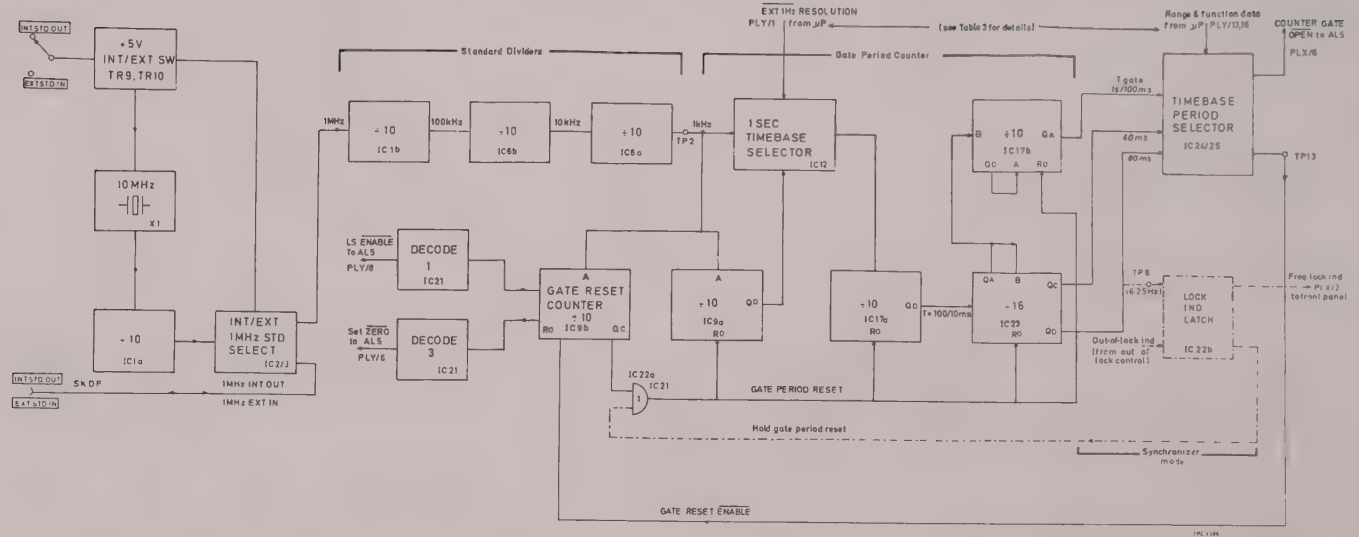


Fig. 30a Counter time base (AL4)

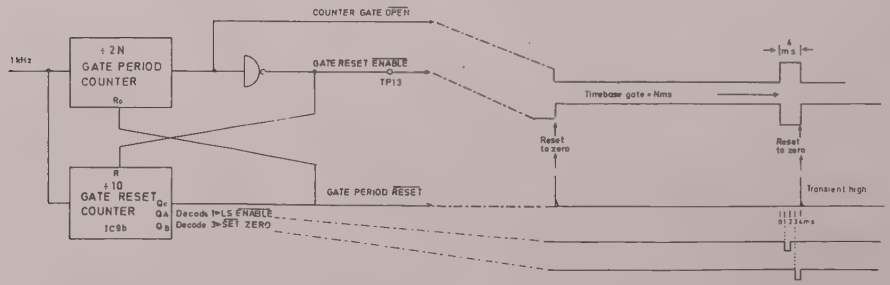


Fig. 30b Simplified counter time base (AL4)

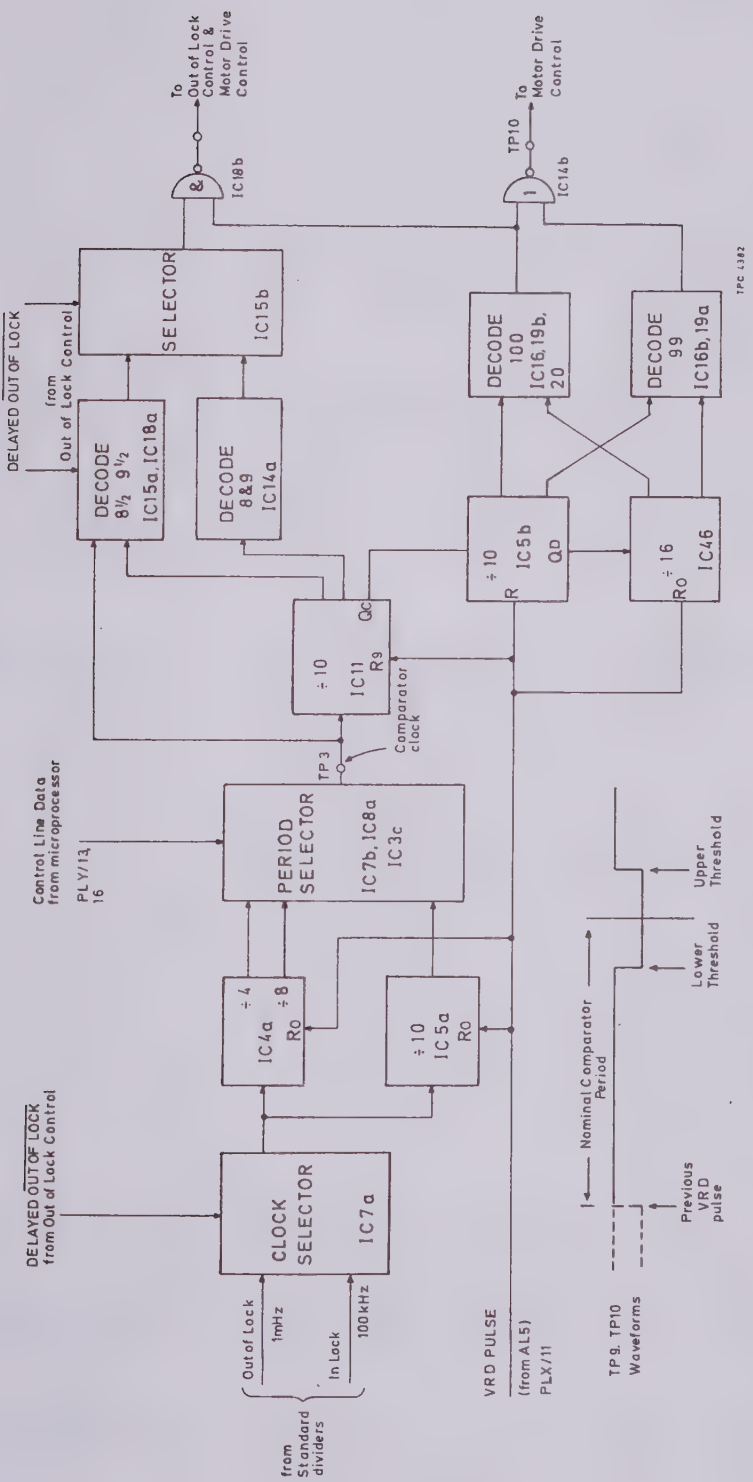


Fig. 31 Period comparator threshold generator (AL4)

Ranges 1-6, Resolution 10 Hz, VRD period 100 ms.

Ranges 7,8, Resolution 100 Hz, VRD period 40 ms.

Range 9, Resolution 100 Hz, VRD period 80 ms.

If the signal frequency is less than the programmed frequency the VRD period increases, and vice-versa relative to the locked state. Small discrepancies between signal and programmed frequency are corrected by electrical fine tuning via the phase detector. Larger errors can only be corrected by coarse tuning the main oscillator through the motor drive. The period comparator continuously monitors the VRD period and, via the out-of-lock control circuitry, activates the motor drive control circuitry.

190. When the signal is locked the period comparator threshold is set at ±0.1%, if the programmed frequency is changed so that the VRD period lies outside this limit then the control circuit assumes an out-of-lock state. In the out-of-lock state AL5 produces VRD PULSES at 10 times the normal rate (see out-of-lock state AL5 paragraph) the faster data rate gives more precise motor drive control. The period comparator automatically adapts to the faster VRD PULSES and sets the threshold at ±0.05%. Thus the motor will drive the main oscillator tuning until the signal frequency is within ±0.05% of the programmed frequency.

191. Threshold generator. The appropriate comparator clock period at TP3 is derived from the 100 kHz or 1 MHz standard by frequency division as determined by the selectors IC7 and IC8a, these are shown in Table 8 below.

TABLE 8 PERIOD COMPARATOR THRESHOLD GENERATOR (AL4)

Frequency range	*Control lines PLY/13 Range 9 ON*	*PLY/16 100Hz RES*	*Delayed 0.0L*	*Clock period at TP3*	*Nominal comparator period*	*TP9 threshold*	*TP10 threshold (nominally ±1%)*
1-6	High	High	High	100µs	100ms	±0.1% = ±100µs	-1.1ms + 0.9ms
1-6	High	High	Low	10µs	10ms	±0.05% = ±5µs	-110µs + 90µs
7,8	High	Low	High	40µs	40ms	±0.1% = ±40µs	-440µs + 360µs
7,8	High	Low	Low	4µs	4ms	±0.05% = ±2µs	-44µs + 36µs
9	Low	Low	High	80µs	80ms	±0.1% = ±80µs	-880µs + 720µs
9	Low	Low	Low	8µs	8ms	±0.05% = ±4µs	-88µs + 72µs

192. The comparator clock frequency is divided down in IC11 (÷10), IC5b (÷10) and IC4b (÷16). IC16 and IC19 decode when counter IC5b and IC4b registers 99 and 100, forcing TP10 low. Now each VRD PULSE resets all the counters of the period comparator to zero except IC11 which is reset to 9, so that after 989 to 999 clock pulses following reset the 99 detector is activated, and 999 to 1009 following reset the 100 detector is activated, giving the nominal ±1% threshold at TP10, see Table 8.

193. IC14a decodes when counter IC11 registers 8 and 9, when this is ANDed with the decode 100 output TP9 goes 'low' 999 to 1001 clock pulses following reset. Hence the nominal ±0.1% threshold at TP9.

194. IC15a and IC18a decodes when counter IC11 registers between 8½ and 9½, when this is ANDed with the decode 100 output then TP9 goes low 999½ to 1000½ clock pulses following reset to give the nominal ±0.05% threshold at TP9. (Note that the occurrence of the VRD PULSE initiates a new count cycle and resets TP9 and TP10 high).

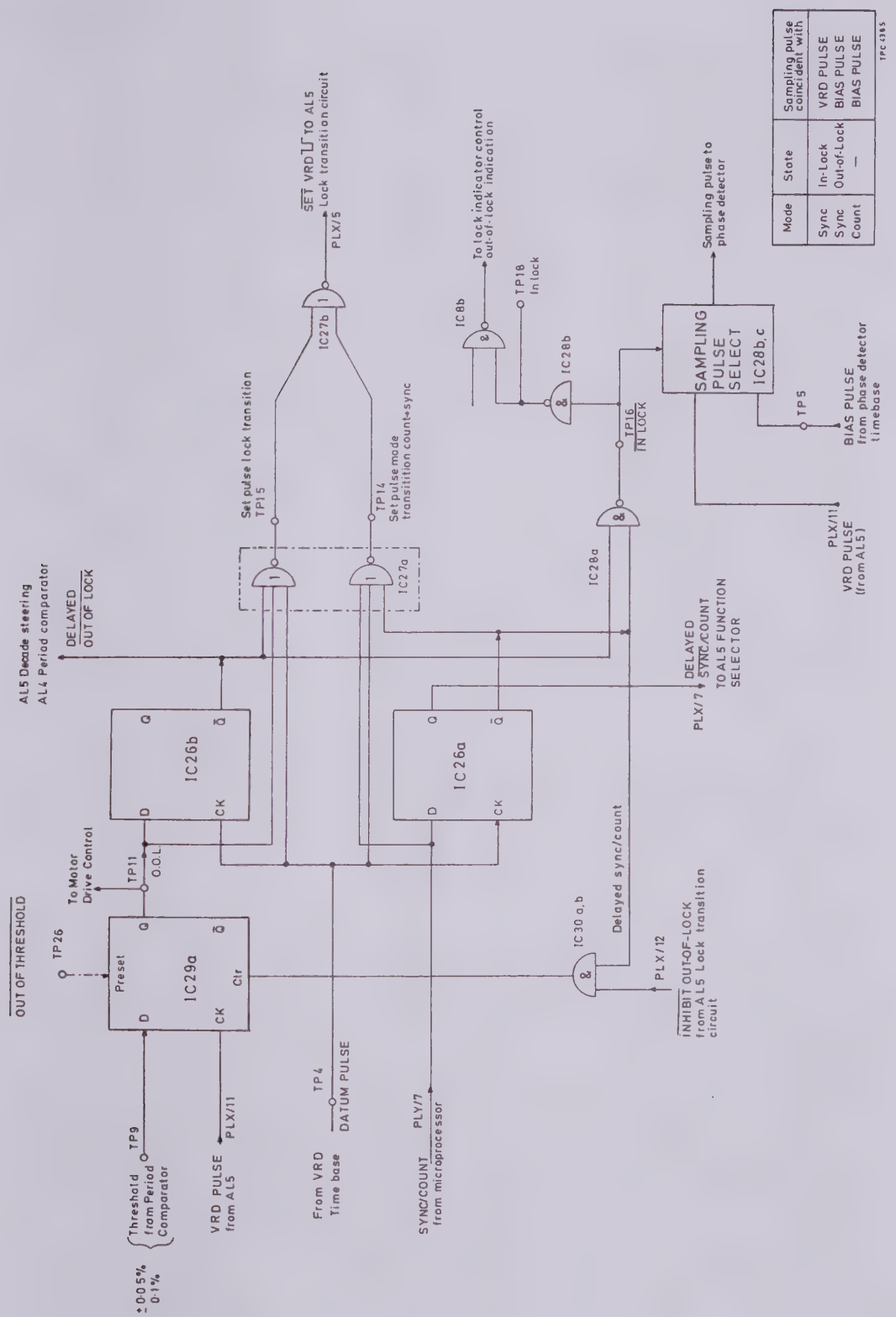
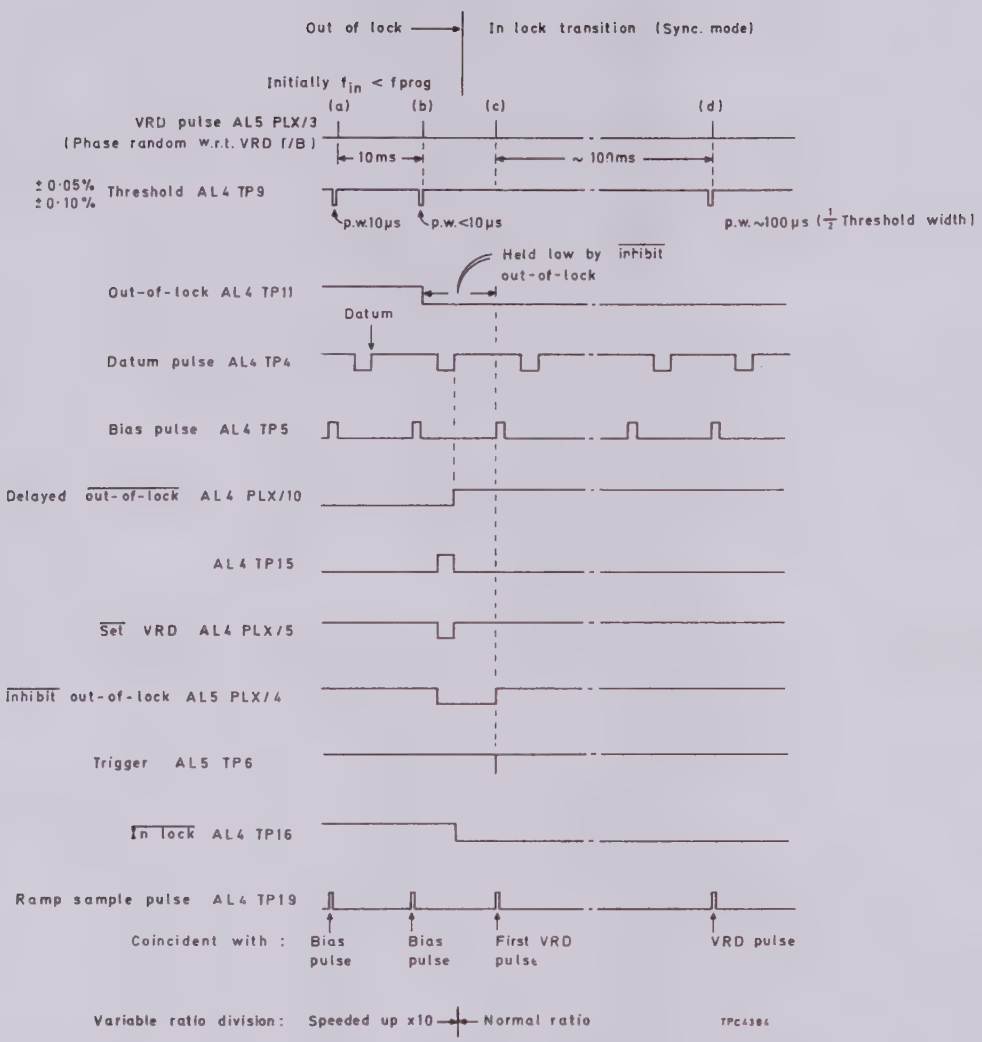


Fig. 32 Out-of-lock control (AL4)



VRD Pulse : (a) Falls outside 0.05% threshold, period comparator registers out-of-lock

(b) Falls inside 0.05% threshold, period comparator registers in-lock

(c) Synchronized to Bias Pulse, period comparator forced to in-lock by Inhibit out-of-lock line

(d) First pulse at normal division ratio falls inside 0.1% threshold } Period comparator registers in-lock

Fig. 33 Out-of-lock control, timing waveforms (AL4/AL5) (Ranges 1-6 illustrated)

Out-of-lock control - see Fig. 32

195. In the Synchronizer mode the out-of-lock control circuit monitors the VRD period in relation to the comparator threshold to determine whether the oscillator frequency is locked, setting TP11 'low', or out-of-lock, setting TP11 'high'. The circuit incorporates a delaying function so that certain control lines may be switched in sequence, these are DELAYED $\overline{\text{OUT-OF-LOCK}}$, DELAYED $\overline{\text{SYNC}}$/COUNT and $\overline{\text{IN LOCK}}$ (TP16), the latter controls the phase detector input and the lock indicator. The circuit also generates a $\overline{\text{SET}}$ VRD pulse which is required by the VRD of AL5 in its transition from the unlocked or out-of-lock state to the locked state, timing waveforms are shown in Fig. 33.

196. The narrow threshold waveform at TP9 is fed to the data input of flip-flop IC29a which is clocked by the VRD PULSE (see Fig. 32). If this pulse occurs within the comparator threshold then TP9 will be 'low', so that the flip-flop output at TP11 assumes a low state which is indicative of the locked state. If the VRD pulse occurs outside the comparator threshold then TP9 will be 'high' so that TP11 assumes a high state (out-of-lock). IC26 is a dual flip-flop clocked by the DATUM PULSE (TP4), change of data input is delayed at the output until the positive edge of the DATUM PULSE occurs. The delayed data lines are DELAYED $\overline{\text{OUT-OF-LOCK}}$ which is fed to AL4 period comparator and AL5 decade steering via PLX pin 10, and DELAYED $\overline{\text{SYNC}}$/COUNT which is fed to AL5 function selector via PLX pin 7. IC27 gates the control lines to produce a 2 ms $\overline{\text{SET}}$ VRD pulse for AL5 transition circuit via PLX pin 5 whenever there is an out-of-lock to in-lock or Count to Sync mode transition.

197. $\overline{\text{IN LOCK}}$ (TP16) controls gate IC28 selecting the input to the phase detector. The phase detector determines the main oscillator fine tuning voltage. The VRD PULSE is fed to the phase detector only when the circuit is in lock in the Sync mode, i.e. when $\overline{\text{IN LOCK}}$ is 'low'; in this state the front panel LOCK indicator is lit continuously.

198. $\overline{\text{INHIBIT}}$ OUT-OF-LOCK line clears flip-flop IC29a throughout AL5 unlock (or out-of-lock) to lock transition, thereby preventing TP11 assuming a spurious 'high' state. In the Unlock mode, DELAYED SYNC/$\overline{\text{COUNT}}$ is 'low' which clears IC29a forcing TP11 into a low state. Transition waveforms are shown in Fig. 33.

Motor drive control - see Fig. 34

199. This circuit determines the state of the motor drive control lines. In the Unlock mode, or when locked in the Synchronizer mode, TP11 is low, forcing MOTOR DRIVE $\overline{\text{ENABLE}}$ at IC18c 'high' thereby inhibiting the motor drive. In the Synchronizer mode whenever TP11 goes 'high' (out-of-lock) then DRIVE $\overline{\text{ENABLE}}$ goes low and the motor actuates except when TP23 is low (see later paragraphs).

200. The main oscillator coarse tuning is such that motor clockwise rotation decreases the oscillator frequency. The motor direction circuit compares the actual signal frequency with the required programmed frequency by examining the phase between the VRD PULSES and the narrow threshold limits of waveform TP9.

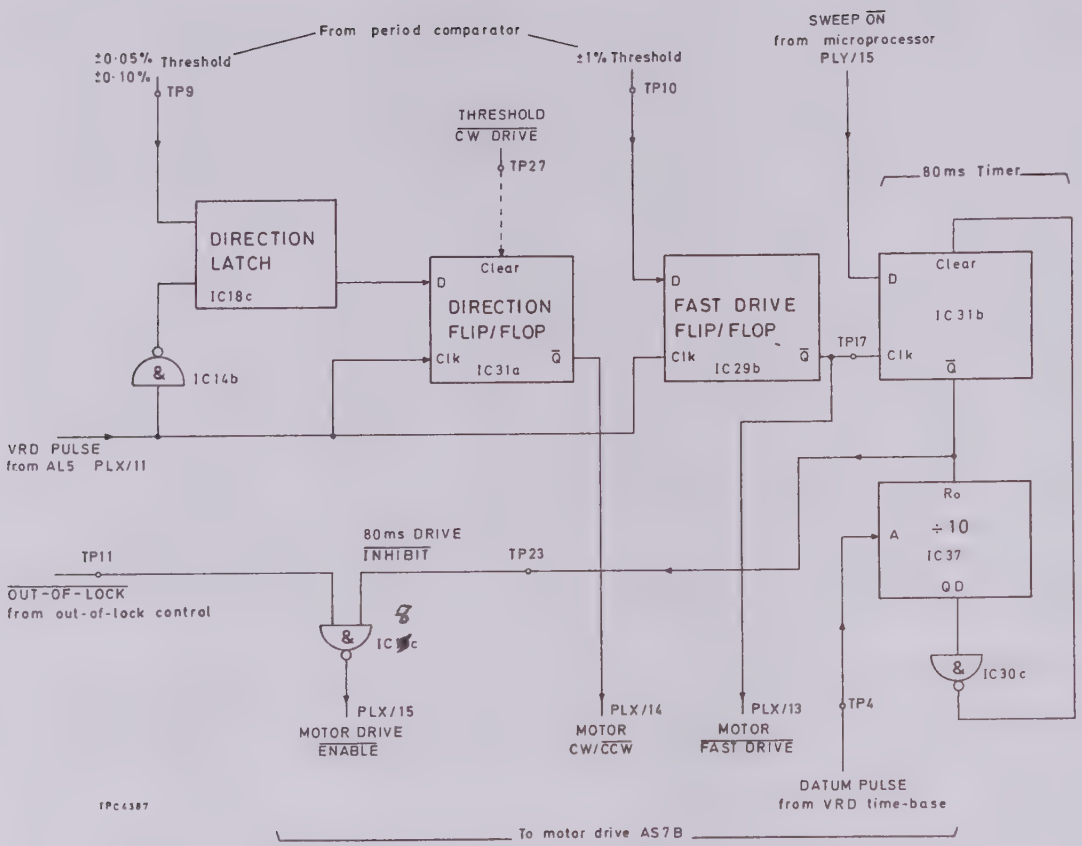


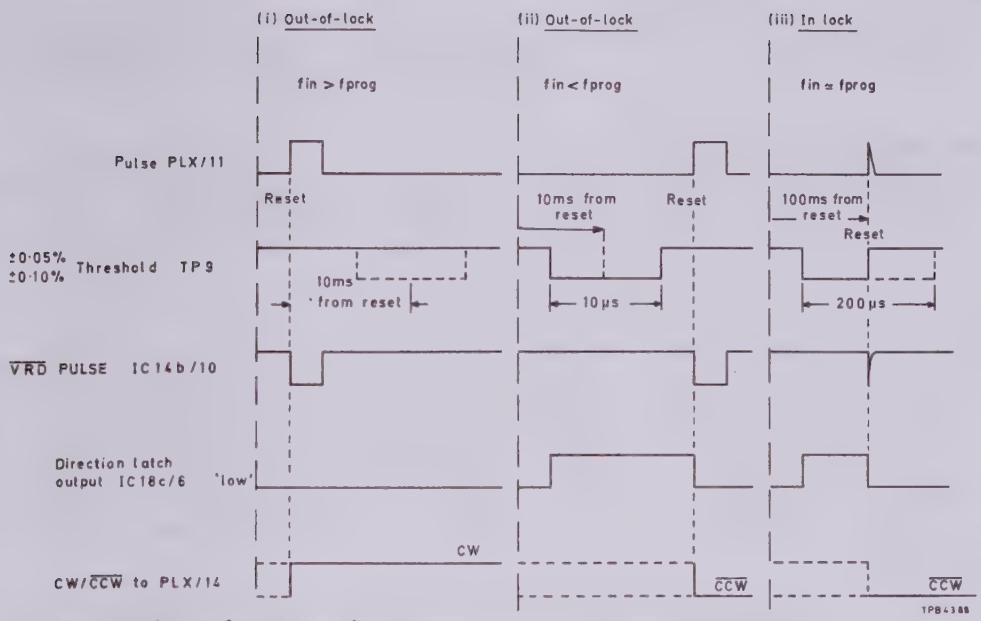
Fig. 34 Motor drive control (AL4)

201. Direction circuit - see Fig. 35

(i) When signal frequency is greater than the programmed frequency each VRD PULSE occurs before the threshold waveform TP9 can go low. The output of the direction latch remains 'low', so that $\overline{Q}$ output of the direction flip-flop IC31a clocks into the high state, i.e. MOTOR CW/$\overline{\text{CCW}}$ line is high thereby tuning the main oscillator to a lower frequency.

(ii) When the signal frequency is less than the programmed frequency each VRD PULSE occurs after the threshold waveform TP9 has set the direction latch into the 'high' state. The VRD PULSE clocks the $\overline{Q}$ output of the direction flip-flop 'low', i.e. MOTOR CW/$\overline{\text{CCW}}$ is low thereby tuning the main oscillator to a higher frequency.

(iii) When VRD PULSES occur within the threshold limits the MOTOR CW/$\overline{\text{CCW}}$ line is set 'low' as in (ii), but the motor drive is not enabled.



Note... Motor clockwise rotation decreases osc. freq.
Motor counter-clockwise rotation increases osc. freq.

Fig. 35 Direction circuit timing waveforms (AL4)
(Ranges 1-6 illustrated)

202. Motor fast drive control. The circuit compares the phase of VRD PULSES with the ±1% threshold waveform TP10. If VRD PULSES occur within the ±1% threshold, the $\overline{Q}$ output (TP17) of the fast drive flip-flop is clocked 'high' so that the MOTOR $\overline{\text{FAST DRIVE}}$ is 'high'. If the VRD pulses occur outside the ±1% threshold limits the fast drive flip-flop is clocked so that MOTOR $\overline{\text{FAST DRIVE}}$ is low.

203. 80 ms Drive Inhibit circuit - see Fig. 34. In the normal Synchronizer mode the motor is stopped for a 70-80 ms interval in the transition from fast to slow drive, preventing overshoot. The positive-going edge of TP17 waveform clocks flip-flop IC31b causing DRIVE $\overline{\text{INHIBIT}}$ line, TP23, to go 'low' thus disabling the motor drive. Decade counter IC37 is thereby enabled to count up to 8 at 100 Hz rate after which flip-flop IC31b is cleared and TP23 goes 'high' removing the Drive Inhibit. In the Sweep mode TP23 remains high, so that the motor drive is continuous until the main oscillator is tuned within ±0.05% of the required frequency.

Phase detector - see Fig. 36

204. The phase detector is a ramp sample and hold configuration which converts the phase of an input pulse into a voltage which fine tunes the main oscillator. The p.r.f. of the ramp waveform is tied to the frequency standard. In the Unlock or Counter mode of operation, TP16 ($\overline{\text{IN LOCK}}$) is 'high', BIAS PULSE (TP5) is selected as input to the phase detector. This causes the centre of each ramp to be sampled so that the phase detector output is a constant voltage. The foregoing applies when motor tuning (out-of-lock) is in the Synchronizer mode or Sweep mode.

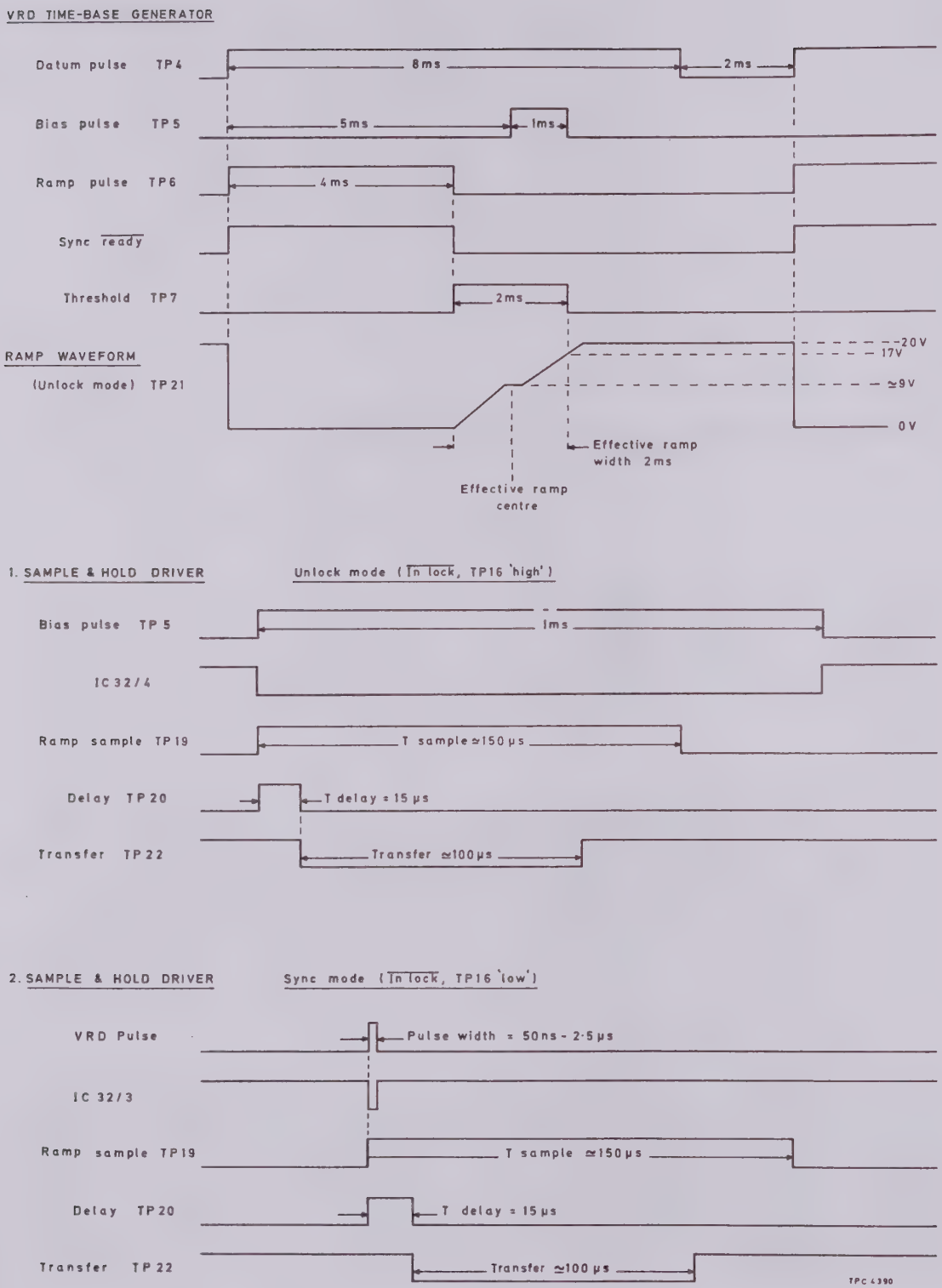


Fig. 36 Phase detector timing waveforms (AL4)

205. When in lock in the Synchronizer mode (TP16 'low') the VRD PULSE from AL5 is selected as the input to the phase detector and this controls the main oscillator fine tuning as part of the feedback loop.

206. Phase detector time base. IC10 and IC13 produces waveforms associated with the phase detector, by decoding the output of decade counter IC10 stepped at a rate of 1 kHz. The sample and hold driver consists of monostables IC32, IC33 and IC34 which produce waveforms determining the ramp sample and hold sequence - see Fig. 36.

207. Ramp generator. TR4, together with R12 and R13 form a constant current source, preset to approximately 10 mA. C47 is the ramp capacitor, with TR5 on and TR7 off TP21 ramps up with a constant slope of 10 V/ms approximately until clamped at 20 V by D1. The ramp start is controlled by the RAMP PULSE TP6. When TP6 is 'high', TR1 is held on so that C47 is discharged and TP1 sits at 0 V. When TP6 goes 'low' TP21 ramps up until maximum level is reached where it remains until reset to 0 V when TP6 goes high again.

208. Sample and hold circuit. The cycle of operation begins when a pulse occurs at the phase detector input, triggering monostable IC32. TP19 goes 'high' for approximately 150 µs, this turns TR3 on and TR5 off, so that the voltage at TP21 stops ramping and is held constant for 150 µs. After a 15 µs delay TP22 goes 'low' turning TR6 off and TR7 on for approximately 100 µs. In this state C47, the ramp capacitor and C55, the storage capacitor, share their charge; then TP22 returns high causing TR7 to turn off, isolating the voltage stored across C55. TP19 now returns low causing TR5 to turn on so that TP21 continues to ramp up. After a number of repeats of the operation cycle a state of equilibrium is reached in which the voltage across the storage capacitor equals the voltage sampled on the ramp, so that no further correction is applied to the output voltage which now remains stable. C62 counteracts the very small proportion of switching waveform fed to the output via TR7 inter-electrode capacitance.

209. Output stage. In order to preserve the voltage stored across C55, it is buffered from the f.m. drive circuits in AS5 by source follower TR8a. TR8a source load is a 2 mA constant current source consisting of TR8b and R19. IC38 is wired as a bootstrap circuit to limit TR8a drain/source voltage to about 8 V, this minimizes dissipation in TR8a and reduces gate leakage current to negligible proportions when the drain current is high.

Threshold detector - see Fig. 37

210. When operating in the Synchronizer mode with frequency locked, it is possible to key in successive Δf increments of less than 0.1% of frequency so that each new frequency is obtained by electrical fine tuning. In this way the phase detector output will approach one or other of the ramp limits and it is necessary to detect when the VRD PULSES fall outside the ramp threshold. Threshold waveform TP7 is 'high' during the effective ramp width, and this waveform is fed to the data input of flip-flop IC35 which is clocked by the sample and hold driver. When within the threshold, flip-flop Q outputs are 'high' which maintains OUT OF THRESHOLD (TP25) 'high' and CW DRIVE (TP27) 'high'.

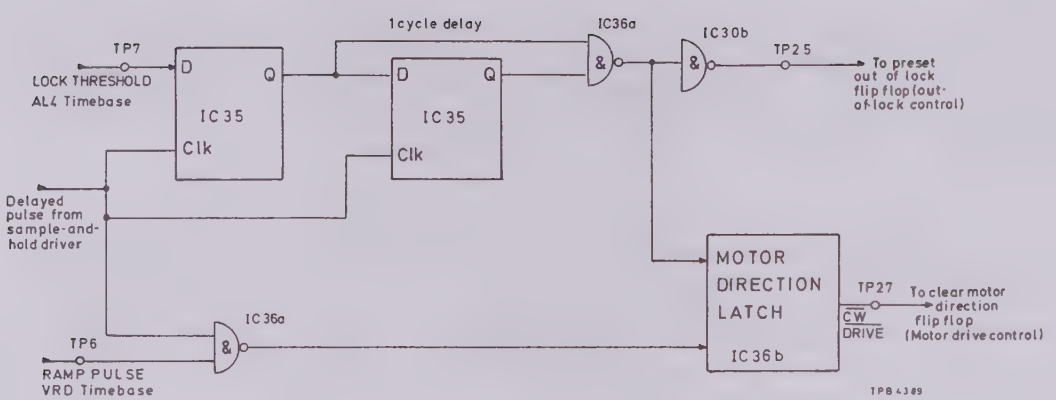


Fig. 37 Threshold detector (AL4)

211. When a VRD PULSE occurs outside the threshold, TP7 is 'low' so that flip-flop Q outputs are clocked successively 'low' causing the $\overline{\text{OUT-OF-THRESHOLD}}$ (TP25) to go 'low'. This presets IC29a to register out-of-lock and actuates the motor drive.

212. If the clock pulse occurs before the ramp starts, then RAMP PULSE (TP6) is 'high', IC36a output sets the motor direction latch so that $\overline{\text{CW DRIVE}}$ (TP27) goes 'low' thereby clearing flip-flop IC31 to force MOTOR CW/$\overline{\text{CCW}}$ line 'high'. Thus the motor drives in the correct direction to reduce frequency.

Lock Indicator circuit - see Fig. 38

213. The Lock Indicator circuit controls the illumination of the front panel LOCK indicator. In the Manual (Count) mode of operation the DELAYED $\overline{\text{SYNC}}$/COUNT being 'high' forces the FREQUENCY LOCK IND line 'low', (front panel lock indicator is off). When in lock in the Synchronizer mode the gate period counter is held reset, FREQUENCY LOCK IND line is high (front panel LOCK indicator is on). When out-of-lock in the Synchronizer mode the gate period counter is enabled producing a 6.25 Hz square wave at TP8, this toggles the FREQUENCY LOCK IND line so that the front panel LOCK indicator flashes at a rate of 6.25 Hz whenever the main oscillator is coarse tuned.

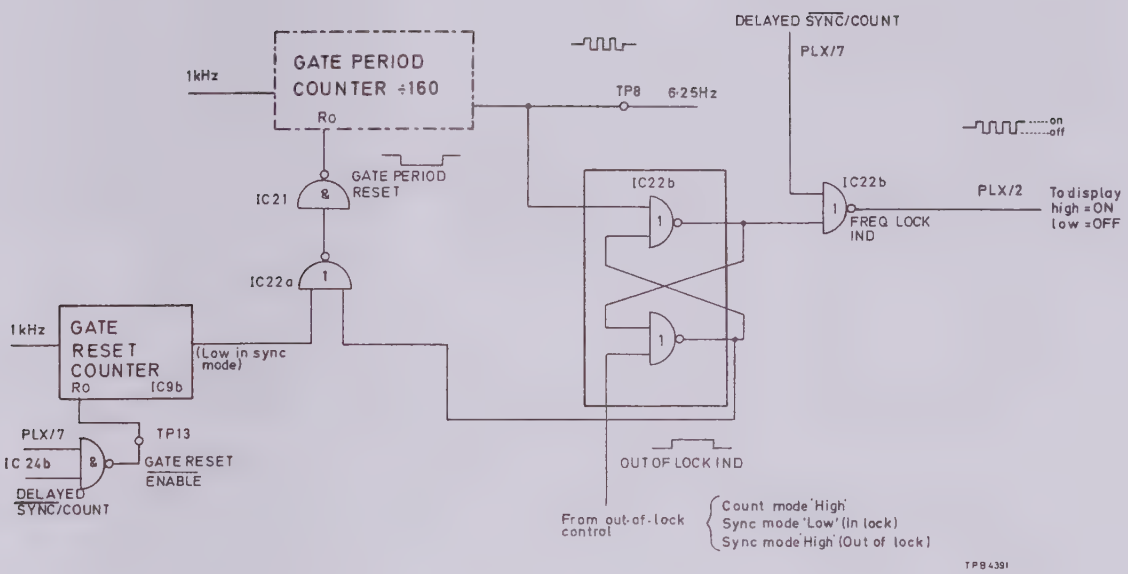


Fig. 38 Lock indicator control (Synchronizer mode) (AL4)

DISPLAY (AL1)

Circuit diagram : Chap. 7, Fig. 7

214. The function of this board is to provide all the display showing on the front panel. With the exception of IC1 and IC14, type 5082-7611 seven-segment display units are used. Each has an array of eight red l.e.d's with common anodes which are optically magnified to form seven individual segments plus a decimal point on the right-hand side, if needed.

215. IC1 and IC14 are type 5082-7616 displays and although the package contains six red l.e.d's only three are utilized. These indicate the numeral one, and the negative polarity sign. The negative sign indicates a minus shift of frequency when operating in the Δf mode or a negative dBμV r.f. output level selection, positive polarity is always inferred and therefore not displayed.

216. Diodes D1 to D35 inclusive are all type HLMP 0301 solid state red lamps. Such words as PULSE and LIMIT are illuminated by two l.e.d's in parallel, these have their current limiting resistors fitted on the display board AL1. The remainder are fitted on the display drive board AL2.

DISPLAY DRIVE (AL2)

Circuit diagram : Chap. 7, Figs. 8 and 9

217. Modulation and carrier level information to be displayed by the Display Unit AL1 is outputted from the microprocessor on a 4-line data bus. The b.c.d. data for each digit is presented in turn and directed to the correct display position by an address bus and latches. This board contains the latches and display decoder/drivers.

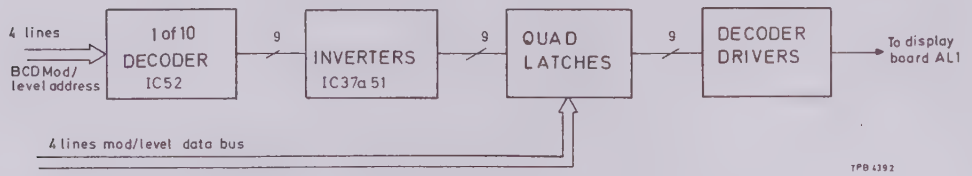


Fig. 39 Modulation and level display drive (AL2)

218. Each latch stores data until enabled via an inverter coupled to a 1 of 10 decoder, IC52. When the latch is enabled, data is captured whilst present on the data bus and fed via a decoder/driver to the 7-segment decimal display on AL1. Modulation and carrier level data arrives on PLE pins 3, 4, 11 and 12. The b.c.d. address arrives on PLE pins 5, 6, 9 and 10.

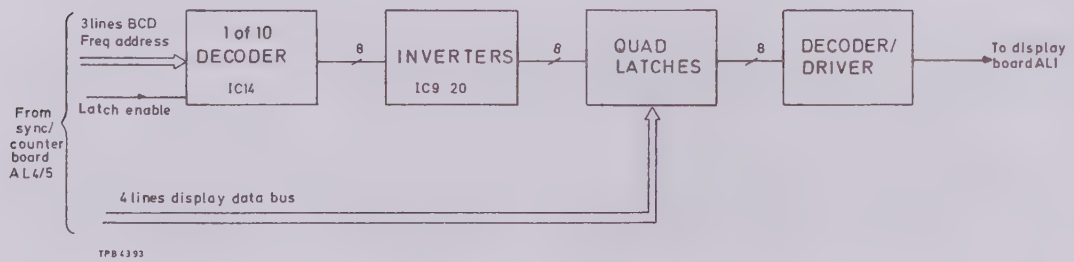


Fig. 40 Carrier frequency display drive (AL2)

219. A second data and address bus pair is used for the carrier frequency display, driven directly by the synchronizer/counter board AL4/5; here the data arrives on PLC pins 2, 3, 12 and 13 and the address on PLC pins 5, 6 and 10. Only three lines are needed to code the 8-digit latches; however an additional latch enable line on PLC pin 11 is used (LATCH GATE $\overline{\text{OPEN}}$) to delay latching until both data and address are correct. When both are synchronized one of the NOR gates in IC9 or IC20 output a level '1' instruction to the appropriate latch.

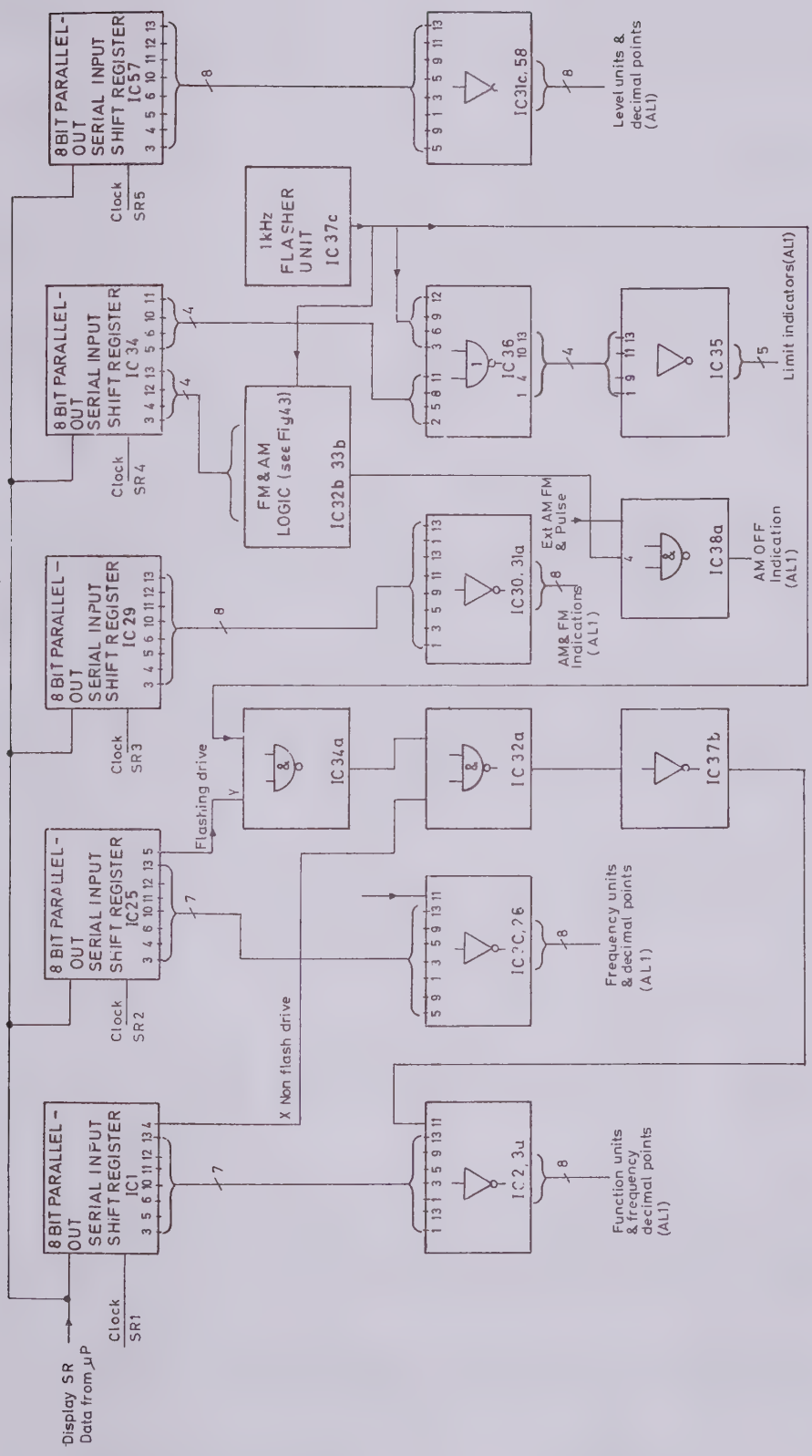


Fig. 41 Parallel-out-serial-input registers (AL2)

8 bit parallel-out-serial-input registers - see Fig. 41

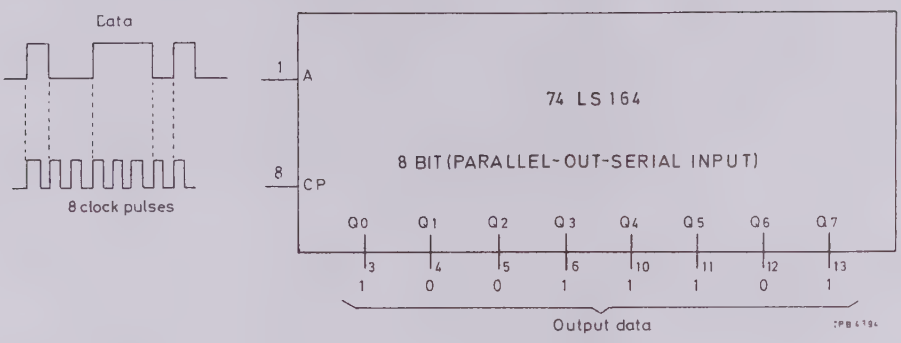


Fig. 42 Parallel-out-serial-input data (AL2)

220. Serial information is also fed from the microprocessor via PLD pin 9 on a common shift register data line to a number of 8-bit parallel-out-serial-in registers. These supply the display unit AL1 with the supplementary front panel indications such as decimal points, Δf, sweep, limit indications etc.

221. The serial data is applied simultaneously to all the registers at pin 1,A - see Fig. 42, and is synchronous with clock pulses fed to the CP input at pin 8 from the microprocessor. Only one of the five register clocks SR1 to SR5 is pulsed by the microprocessor at a time, so only that register is loaded with data. After its 8 bits have been loaded, the following 8 bits are loaded into the next register when its clock line receives 8 clock pulses. Whenever any of the 40 bits of data needs to be changed, all 40 are reloaded.

222. Each clock pulse on the CP input pin 8 shifts data in the register one place to the right and enters into the left position Q0 (pin 3), the current data on data input A (pin 1). The 8 register outputs are inverted and fed to the indicator l.e.d's on the display unit AL1.

AM or f.m. ON/OFF lamp drive logic

223. The logic for both f.m. and a.m. is similar, therefore only the a.m. logic is considered. There are four inputs - see Fig. 43a and b. These are as follows:-

(a) A 1 Hz square wave to provide a flashing indication when unwanted conditions exist.

(b) An AM LEVEL $\overline{\text{ERROR}}$ instruction which comes from AS3 modulation leveller board to indicate by flashing the AM OFF l.e.d. that the modulation will not be calibrated.

(c) A latched bit from the microprocessor to give a flashing AM OFF indication when the requested a.m. modulation is invalid i.e. when the output level is at +126 dBμV or greater.

(d) A further latched bit to give a steady AM OFF indication when a.m. is not selected.

224. Fig. 43a shows the operation of the logic circuit IC33b and IC38a during the AM OFF condition, IC38a outputs a steady '0' AM OFF indication.

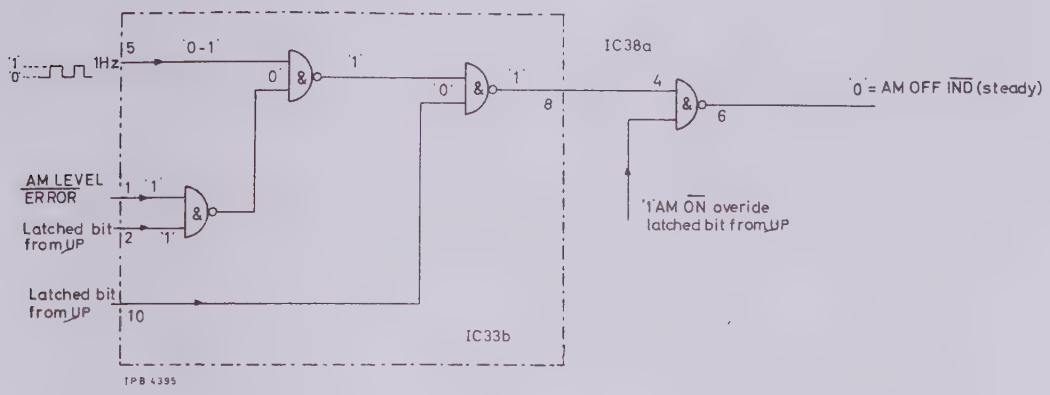


Fig. 43a AM OFF logic (AL2)

225. Fig. 43b shows the same circuit operating when an a.m. level error exists and the input at (b) changes from level '1' to '0' level. Similarly a change to '0' level at input (c) would also give the same result, that is a flashing AM OFF indication.

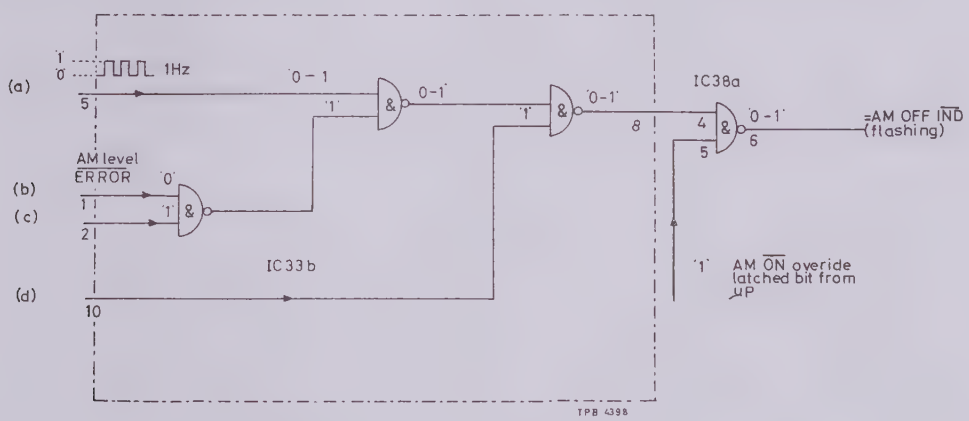


Fig. 43b AM level error logic (AL2)

MICROPROCESSOR SYSTEM (AL3)

Circuit diagram : Chap. 7, Fig. 10

226. The control system inside 2017 is made up of an 8085A microprocessor, 8k bytes of ROM (program storage), 512 bytes of RAM (work space and instrument storage) and 256 bytes of PROM (FM tracking). Connection between the system and the 2017 hardware is via 8 programmable input/output ports and a GPIB talker/listener integrated circuit.

227. The components and their interconnections are briefly described below. A full description can be found in "MCS 85 Users Manual" published by Intel Corporation.

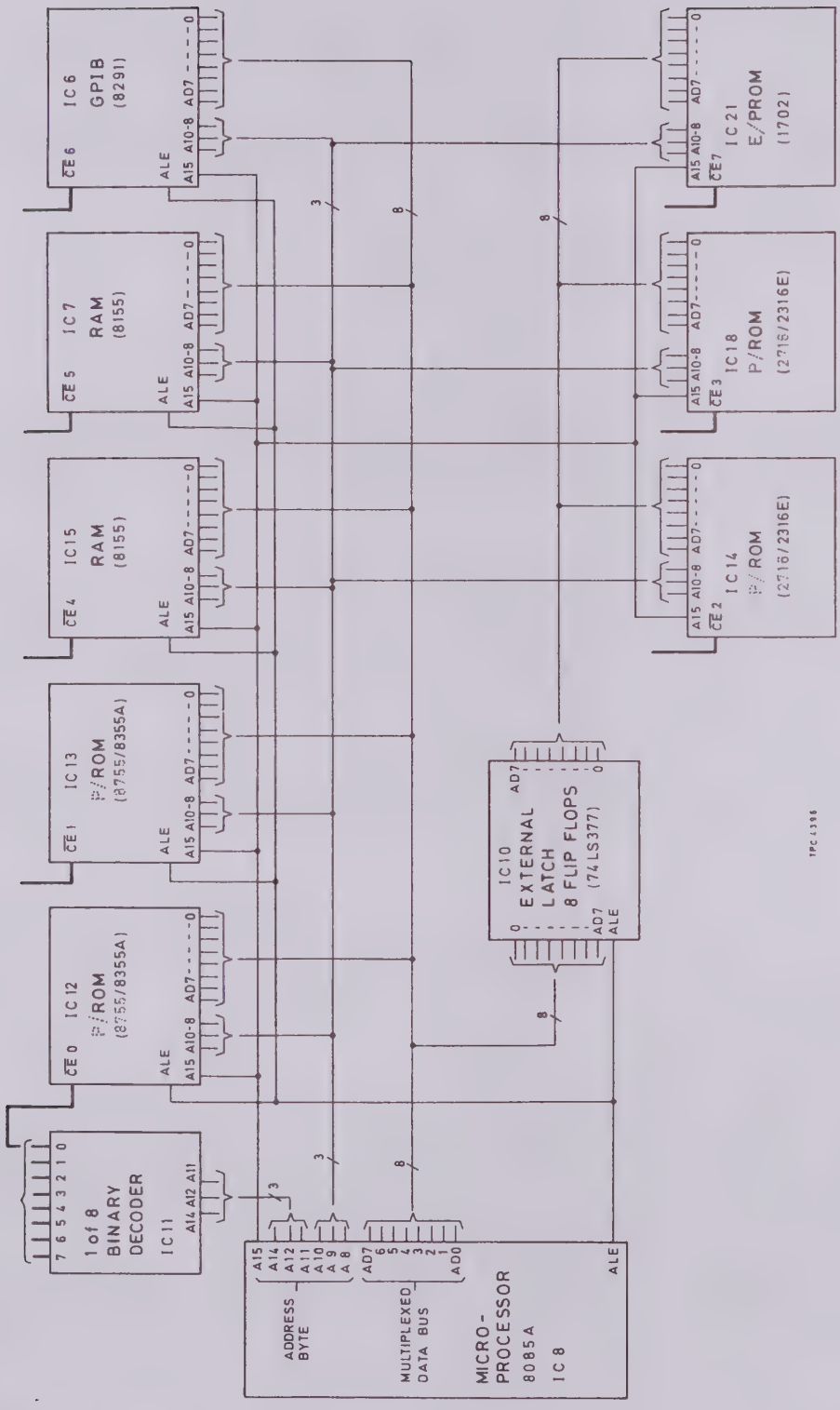


Fig. 44 8085A Microprocessor system (AL3)

228. IC8 (8085A). An 8-bit NMOS microprocessor, with on-chip clock generation, interrupts, and featuring a multiplexed address/data bus. It is compatible with software in the 8080 series, but has two extra instructions available to it, and operates faster.

229. IC12, IC13 (8755A/8355A). 2k byte PROM/ROM (8755A memory is programmable, 8355A is not) with two 8-bit bi-directional input/output (I/O) ports. Its multiplexed address/data bus allows the 8755A/8355A to connect directly to the 8085A.

230. IC14, IC18 (2716/2316E). 2k byte PROM/ROM (2716 is programmable, 2316E is not). This device has conventional, separate, address and data buses, requiring the 8085A bus bars to be de-multiplexed to allow interconnection. This is carried out by the pack of 8 flip-flops, IC10.

231. IC7, IC15 (8155). 256 byte RAM with two 8-bit bi-directional I/O ports and a 6-bit bi-directional port. A programmable timer is included on the I/C but not used in 2017. Its multiplexed address/data bus allows the 8155 to connect directly to the 8085A.

232. IC21 (1702AL). 256 byte PROM with conventional, separate, address and data buses so is connected in the same manner as IC14/IC18 to the 8085A via IC10.

233. IC6 (8291). A GPIB talker/listener integrated circuit, connecting directly to the 8085A, which implement the full IEEE 488 specification for talker/listener devices (no control function).

234. IC11 (P8205). 1 of 8 binary decoder driven by A11, A12 and A14 of the 8085A. This is used to select which of the above ICs is active (only one can be active at any one time). The address assigned to each device is given in Table 9 below.

TABLE 9 PROGRAM ADDRESS DATA

8755A/8355A	IC12	0-7FFH	0-2047	decimal
8755A/8355A	IC13	800H-FFFH	2048-4095	"
2716/2316E	IC14	1000H-17FFH	4096-6143	"
2716/2316E	IC18	1800H-1FFFH	6144-8191	"
8155	IC15	2000H-20FFH	8192-8447	"
8155	IC7	2800H-28FFH	10240-10495	"
8291	IC6	3000H-3700H	12288-14080	"
1702AL	IC21	3800H-38FFH	14336-14591	"

235. Of these devices, the two 8755A/8355A's and the two 2716/2316's are used for the main program (address 0-1FFFH), the two 8155's are used for work space and stores, and the 1702AL for storing the f.m. tracking correction data.

8085A instruction cycle

236. The 8085A operation can be broken down into a sequence of instruction cycles, each of which is made up of one to five read or write operations referred to as machine cycles. The first machine cycle of an instruction consists of reading from ROM the opcode to be executed. During the first clock period the contents of the 16-bit internal program counter appears on the full address bus (AD0-AD7 and A8-A15). Before the removal of the address, the ALE line (address latch enable) operates high and low again, allowing, on the trailing edge, the peripheral devices to latch the complete address. Because IC14/IC18 and IC21 do not have internal latches, IC10 carries out the de-multiplexing function instead.

237. Normally the 8085A would now proceed, during the next clock period, to lower $\overline{RD}$ and read the instruction of code that ROM has placed on the data bus. However, as a precaution against memory not responding in time, a wait state, of one clock cycle, is built in to the 2017's microprocessor system. This is achieved by the dual flip-flops IC10, and mean that after the 8085A has sent out an address, and lowered ALE, there is a pause of one clock period to allow memory to respond with the data.

238. At the end of the wait clock cycle, the opcode is read by the microprocessor from the data bus. The machine cycle finishes with one or more clock cycles during which the 8085A executes the fetched instruction. If the microprocessor has just read the first part of a multi-byte instruction then a further read cycle will be carried out, and depending again on the nature of the instruction, a write cycle may be included.

239. The write cycle, which enables the 8085A to send data to a device (memory or an I/O port), is similar to a read except that after the address (to be written to) has been sent, and ALE lowered, the data to be written is placed on the data bus by the microprocessor and $\overline{WR}$ operating low. A wait state follows, after which the microprocessor removes $\overline{WR}$, and the data, and moves to the next cycle.

240. During an instruction cycle the program counter is incremented so that at the start of the next cycle the address of the next instruction is ready to be sent to the address bus. A jump, sub-routine call or return from a sub-routine is achieved by the 8085A over-writing the program counter to force program away from the next instruction (numerically) but towards the next instruction (logically). The 8085A can perform machine cycles other than "fetch" "read" and "write" but these are not used in 2017.

Input/output

241. 2017 microprocessor uses memory devices that contain I/O functions to economize on board space and the number of ICs utilized. Although physically housed on the same IC as the ROM or RAM the I/O circuitry can be considered as an independent entity. The 8085A allows use of special I/O instructions that assume the I/O devices to be wired 'conventionally'. This is referred to as I/O mapped I/O. However it is possible, by sacrificing some of the 8085A's 16-bit address capability, to wire the I/O so that each port appears to the processor as a memory location. Hence the programmer can, by simply addressing the appropriate 'memory' location, read, or write to, any port. This is referred to as "memory mapped I/O", and, as is more general in its application, is the option used in 2017.

242. A memory chip knows whether a memory location or an I/O port is being addresed by the state of its IO/$\overline{M}$ pin at the time. For "I/O mapping" this is wired to the IO/$\overline{M}$ pin of the 8085A, but for "memory mapping", assuming that only half of the 16-bit address capability is needed, it is usual to connect the memory IO/$\overline{M}$ pin to the A15 address line from the microprocessor. This means that all addresses below 2^{15} (= 32768) will be routed to memory, whereas all those between 2^{15} and 2^{16} will be considered as intended for I/O.

Re-set

243. Although the microprocessor will execute instructions sequentially (except at a jump, etc.), the address of an instruction about to be executed being held on the program counter, it is essential that, at switch-on, something forces the program counter to a known value in order to start the program running correctly. This is achieved by the $\overline{\text{RESET IN}}$ pin 36 on the microprocessor which, connected to the RC network R7 and C8, stays low for a short time after the supply reaches +5 V. This resets the program counter to zero, and causes the RESET OUT pin 3 on the 8085A to go high. RESET OUT is connected to the I/O ports and the GPIB integrated circuit, initializing them at the same time the program starts.

Clock

244. The 8085A does not need an external clock generator. Crystal XL1 is connected directly to pins 1 and 2, and the necessary two-phase clock is produced internally. One phase of the clock appears on the CLOCK OUT pin 37, synchronizing external devices as necessary. Although the crystal frequency is 6.144 MHz there is an internal divider, so the signal at CLOCK OUT is at 3.072 MHz.

LATCHES BOARD (AS2)

Circuit diagram : Chap. 7, Figs. 24 and 25

245. The microprocessor AL3 is contained in a screened box with all external connections carefully filtered. It is therefore undesirable to wire all the 2017 front panel functions and internal controls individually so creating the need for extensive wiring and many additional filter components. The functions and controls have instead been wired direct to the latches board AS2 situated outside the screened box and a total of thirteen filtered lines only are required to interface this with the microprocessor.

246. There are eight octal latches used to store instructions from the microprocessor and four octal flip-flops connected as tri-state gates. The gates are used to select the front panel information to be read by the microprocessor. Latches and gates are accessed to the microprocessor by an 8-bit data bus. A 4-bit address bus is also connected to a 4-16 decoder on AS2 to give twelve discrete enable lines; these are used to enable each of the latches and gates when individually addressed. A further $\overline{\text{ADDRESS VALID}}$ instruction $\overline{\text{OE}}$ is used to introduce a delay in the decoder operation, this allows data normally delayed through the filtered lines to reach the latches board in the correct order.

Circuit description

247. The 4-bit function address is fed from the microprocessor to the 4-16 line decoder IC12 via PLT pins 1, 2, 13 and 14. Data from the microprocessor is fed via PLT pins 3, 5, 6, 7, 9, 10, 11 and 12 to all the latches and gates and the $\overline{\text{ADDRESS VALID}}$ instruction from PLBH pin 3.

248. The inputs to the decoder IC12 are normally held high until the appropriate address is placed on the bus, a wait sequence follows (approximately 1 µs) to allow for the delay subjected by the 1 MHz filters fitted on all lines. After this delay the $\overline{\text{ADDRESS VALID}}$ 'low' instruction enables the 4-16 decoder and the required latch or gate is accessed by one of the decoder's twelve output lines. A wait sequence is also placed between each instruction giving typical input and output sequences as shown in Table 10 below.

TABLE 10 LATCHES BOARD ADDRESS SEQUENCE (AS2)

Input	*Output*
Place address on address bus	Place data on data bus
Wait	Wait
$\overline{\text{ADDRESS VALID}}$ '0' low	Place address on address bus
Wait	Wait
Read data bus	$\overline{\text{ADDRESS VALID}}$ '0' low
Wait	Wait
$\overline{\text{ADDRESS VALID}}$ '1' high	$\overline{\text{ADDRESS VALID}}$ '1' high
Wait	Wait
Remove address	Remove address
	Wait
	Remove data

GPIB (AL3/AG1)

Circuit diagrams : Chap. 7, Figs. 10 and 13

249. The function of the GPIB drive board AG1 is to provide buffering between the general purpose interface bus and the 8291 GPIB handler on the microprocessor board, AL3. As the microprocessor board is located within the screened logic box and all lines from the logic box are filtered, some high speed drivers are needed to operate the filters fast enough to meet the GPIB specifications.

250. For those GPIB lines sending information to the 2017 filter drivers are situated on AG1 and the receivers on AL3. For those carrying information from the 2017 filter drivers are on AL3 and the receivers on AG1.

251. The external controller directs the flow of data on the bus and designates when the 2017 is to send data and when it must receive it. The bus uses 16 signal lines to connect all units of a system in parallel. These lines are sub-divided into data, transfer and interface management buses as shown in Fig. 45 below.

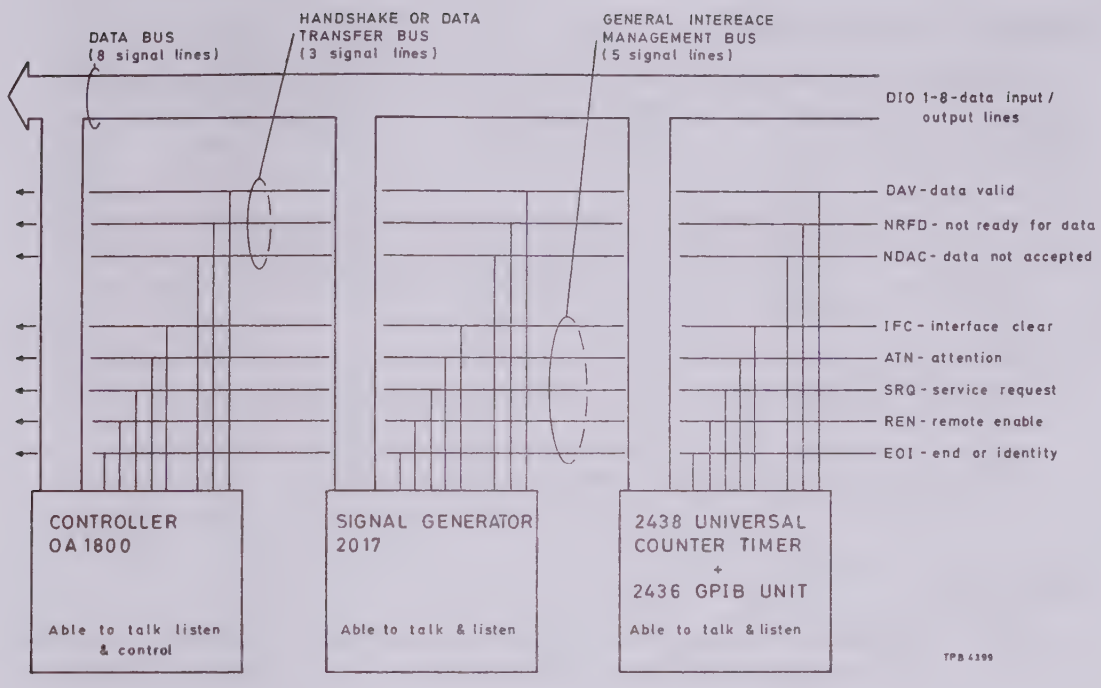


Fig. 45 Interface bus structure (AG1)

Data bus

252. Comprises 8 data input/output lines DIO 1 to 8 and is used to transfer the data (commands, addresses and instructions) in bit parallel, byte serial form.

Interface management bus

253. Manages the orderly flow of data across the interface and consists of 5 wires carrying the following signals:

Interface clear (IFC); sent by the system controller to clear all device interfaces so that they set to an initial condition.

Remote enable (REN); sent by the controller to enable instruments to be placed under remote control.

Attention (ATN); sent by the controller to indicate that an address or command is on the data lines.

End or identify (EOI); an instrument or controller signal sent to indicate the end of a message.

Service request (SRQ); sent to a controller by an instrument to indicate that it needs service e.g. 2017's reverse power protection has tripped.

Handshake or data transfer bus

254. Co-ordinates the flow of data and comprises 3 lines which are used for the handshaking process, by which a talker or controller synchronizes its readiness to send data with a listener's readiness to receive data. The handshake signals are:

Not ready for data (NRFD); asserted (low) by a listener when it is active and not yet ready to receive data. Set high to signal its readiness to receive data, DAV can then be signalled if further data is to be processed.

Data valid (DAV); asserted by a talker to indicate that the data it has placed on the data bus has settled and may be accepted.

Not data accepted (NDAC); asserted by a listener when receiving information from the data lines. Release of the NDAC line tells the data source that new data can be submitted.

Bus operation

255. (i) A sequence of messages may be commenced by the controller asserting IFC on the management bus to set the interface to its initial condition.

(ii) The controller then sets up which instruments are to be listeners by asserting ATN and handshaking the personalized listen address of these instruments over the bus. Similarly the controller designates the talker (only one instrument may talk at a time) by sending its talk address, again with ATN asserted.

(iii) On release of the ATN command (i.e. $\overline{\text{ATN}}$) the talker is then able to place data on the data lines DIO 1 to 8, the transfer of this is controlled by the handshake process and is received by all addressed listeners. The talker typically concludes the sequence by asserting EOI and the controller then resumes control.

(iv) Both the talker and the listeners may be switched by the controller into an inactive state by asserting IFC or sending OTA (other talk address) and UNL (unlisten) on the data bus.

Handshake procedure

256. The handshake is used whenever data is transferred on the bus. When a signal is asserted the function indicated by the line is carried out, e.g. NRFD is asserted to signify the listener's unreadiness to receive data, and unasserted or removed when ready to receive data. A typical handshake is as follows:

(i) Talker (controller) places a byte on the data bus with DAV initially unasserted to show data is not yet valid.

(ii) When all listeners are ready to receive data NRFD is removed with NDAC at this time asserted.

(iii) After a delay to allow the data bus to settle, talker asserts DAV to show data is valid and may be accepted.

(iv) Data byte is transferred, then listeners assert NRFD. When all the listeners have accepted the byte NDAC is removed to signify receipt.

(v) Talker removes DAV, listeners assert NDAC, and the bus reverts to its initial condition ready for the next data byte, a typical cycle is shown below in Fig. 46.

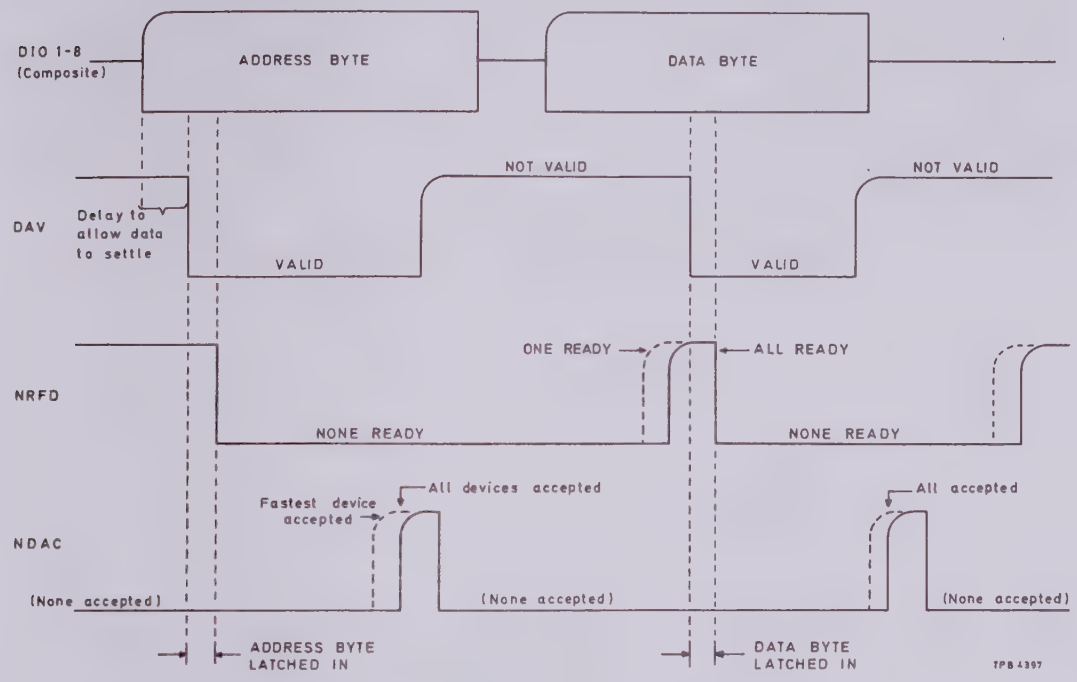


Fig. 46 Handshake procedure

257. Also provided on board AG1 are the GPIB bus terminator loads and the address selection switch.

CHASSIS (A0)

AC pre-regulator and mains selector (AP1) - see para. 265

Circuit diagram : Chap. 7, Fig. 5

258. Pre-regulation of the mains input supply to the main transformer, T1, is achieved by monitoring one of its outputs and switching the supply to the optimum of ten available primary taps by means of triacs. To avoid interference the sequential tap changes may occur only when the mains current passes through zero.

259. The mains is also fed directly to an auxiliary transformer, T2, to operate the pre-regulator circuits. Initially the triac connected to the highest voltage tap is turned on. This ensures that the d.c. regulators are not overvolted and that the least possible current surge occurs should the transformer be magnetized in the wrong direction.

260. The monitored output of T1 is compared with two reference voltages to define a range of output voltage within which a tap change is not required. If the monitored voltage is below this range the next lower tap is selected by decrementing the ten step up-down counter which drives the triacs. Further comparisons take place and the tappings changed until the sense voltage is within the specified limits (maximum time required to move through all ten taps is 200 ms). Subsequent mains voltage changes cause the counter to step up or down whenever the limits are exceeded. A slight amount of hysteresis is built in to the comparator circuits to prevent hunting. These and other control functions are incorporated in a custom LSI integrated circuit, IC3, shown in Fig. 47 below.

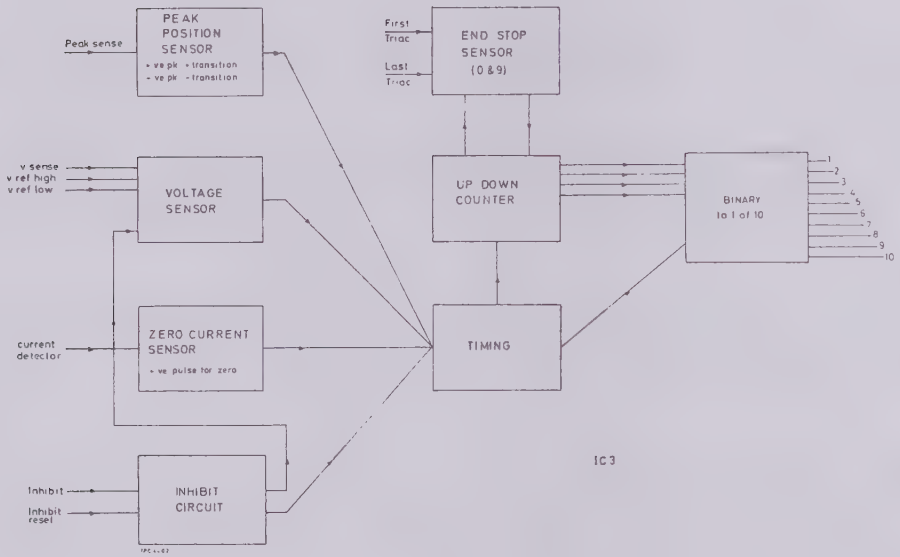


Fig. 47 Pre-regulator simplified block diagram

Circuit description (AP1)

261. The a.c. input is fed through two 2.5 A circuit breakers CB1 and CB2 to the supply switch SE via PLAE and SKAE pins 2 and 6, and returned through SKAE and PLAE pins 1 and 7. The neutral line is connected through PLAR and SKAR pin 26 to the primary windings of T1, and the live line through D1/D2 to the input of all ten triacs. Selection of the required triac is then carried out and the supply connected through PLAK, SKAK, PLAR and SKAR to the required tapping point on transformer T1.

Mains supply range tappings (SKAK)

262. Two sockets covering the voltage supply ranges 94-132 V a.c. and 188-265 V a.c. are provided. The socket appropriate to the required range is inserted into plug PLAK and the socket not required is placed in a stowage position provided on the inside of the rear panel. The panel has an observation window where the supply range voltage in use is indicated on the alternative socket stowed there. The two voltage supply ranges are connected as shown below in Fig. 48.

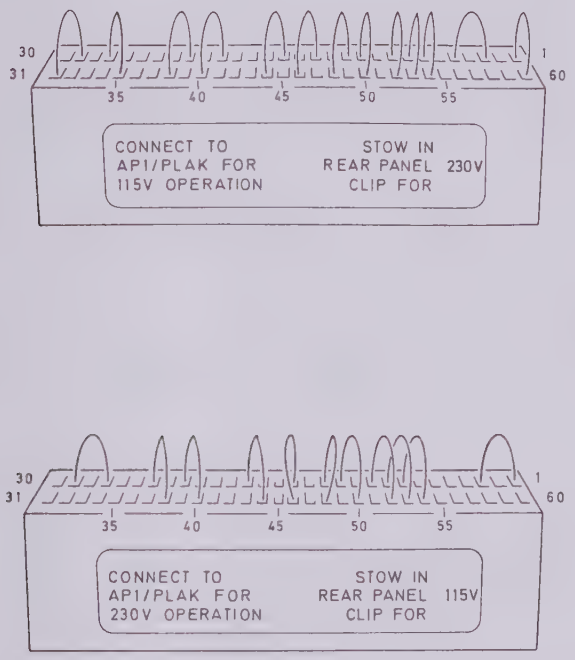


Fig. 48 115 V/230 V mains supply tappings (SKAK)

Zero current sensing (AP1)

263. To ensure that two triacs are never turned on at the same time it is necessary to switch between taps at the zeros of current. Two diodes, D1 and D2, are connected in inverse parallel together with a 100 Ω resistor, R5 in the live side of the mains. Only when the supply current is nearing zero and both diodes are cut off can TR3 turn off, producing the positive-going transition of the current sensor output pulse shown in Fig. 49 below.

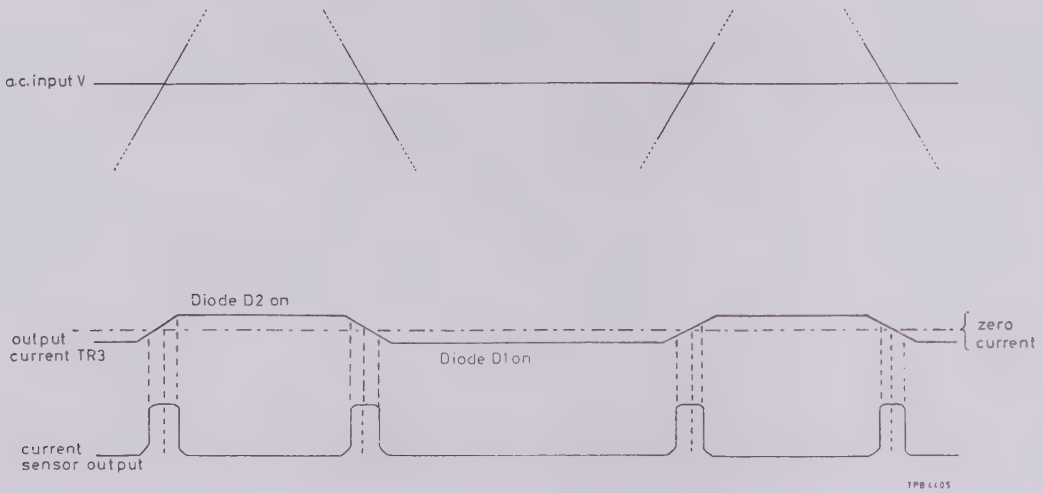


Fig. 49 Current sensor output pulses (AP1)

264. During the time TR3 is turned off the current sense output remains high until the supply current exceeds about 4 mA again. TR3 is then turned on via either TR1 or TR2 and the current sensor output pulse returns to zero.

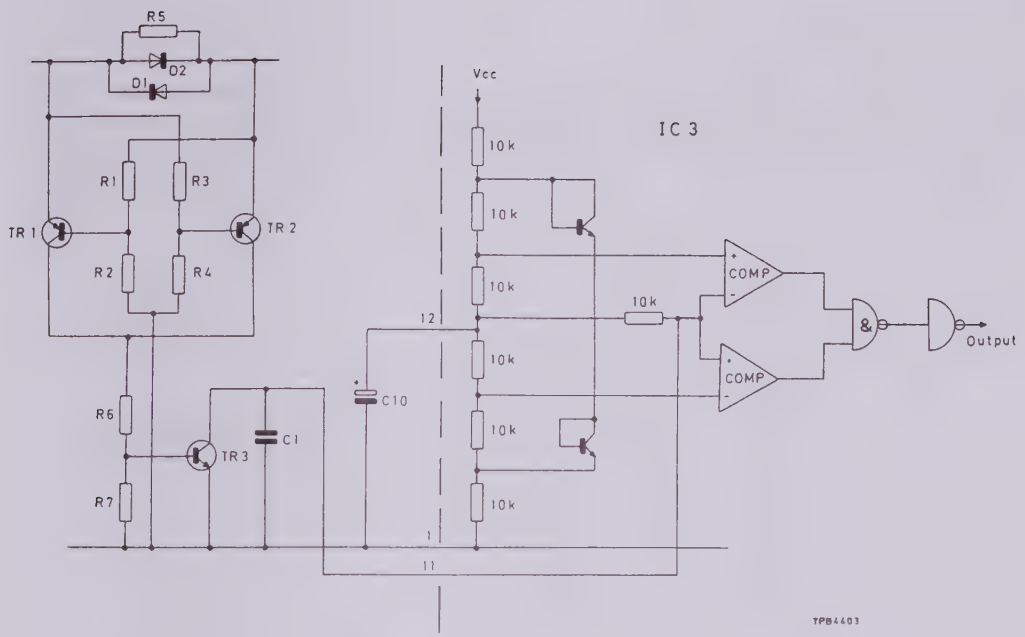


Fig. 50 Zero current sensor circuit (AP1)

Control circuit power supply (AP1) ⚠

265. An auxiliary transformer, T2, is used to give the regulated 5 V supply required by IC2,3 and 4. The 5 V rail is connected to the live line placing these circuits at almost mains potential as shown in Fig. 51 below.

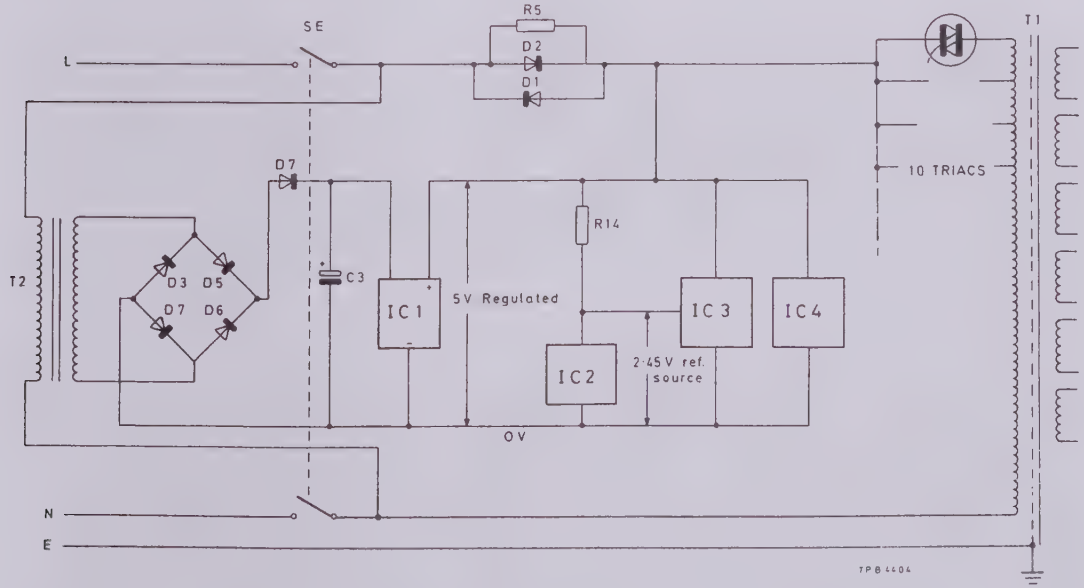


Fig. 51 Control circuit power supply (AP1)

Inhibit circuit (AP1)

266. The inhibit circuit delays the switch on of triacs after a break in the mains supply of more than a predetermined length (approximately 23 ms). This will ensure that no errors result from a low or non-existent pre-regulator power supply.

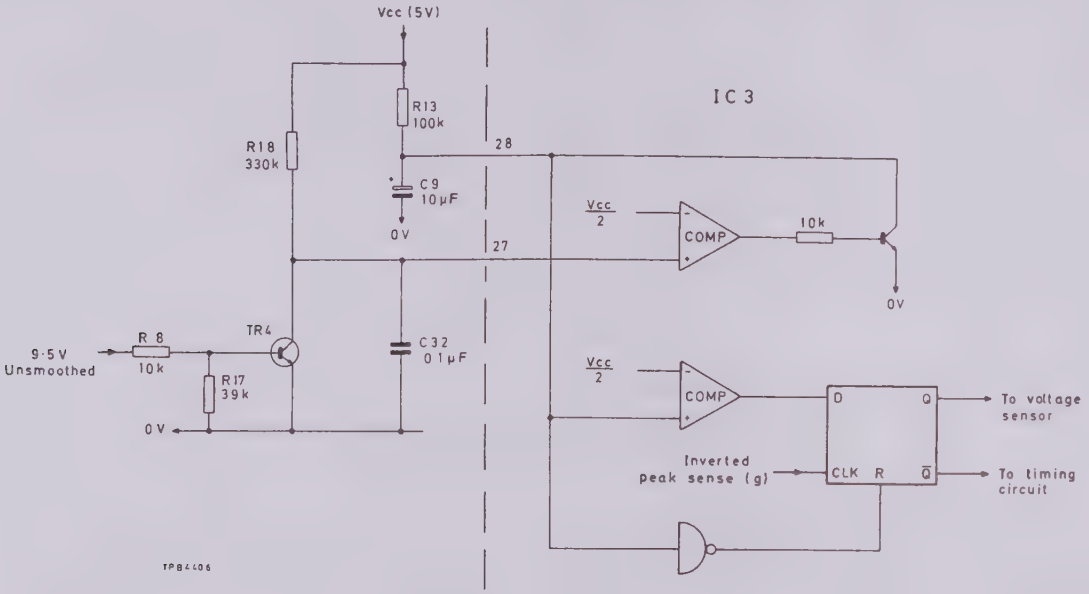


Fig. 52 Inhibit circuit (AP1)

267. During each half cycle of the supply TR4 is turned on via R8 and discharges C32 to 0 V. If the supply is intermittent or missing, the ramp will continue until the comparator within IC3 trips; this in turn causes C9 to discharge and IC3 output is inhibited. When the correct supply is restored C9 recharges and after about one second the bistable within IC3 re-enables the output drive. The same delay is incurred when the instrument is first switched on while the pre-regulator supplies are established.

Voltage sensor (AP1)

268. The voltage sensor is a peak detector circuit, it compares the positive peak voltage of the sense windings on the main transformer, T1, with two reference voltages. Under normal circumstances the peak sense voltage will lie somewhere between the two reference voltages indicating that the main transformer is operating with the correct tapping selected. If the sense voltage exceeds these limits the logic circuit sends a pulse to the up/down counter which will change state at the next zero crossing. Internal logic prevents the counter overflowing. The 2.45 V reference voltage is derived from the 5 V regulated supply by IC2 as shown previously in Fig. 51 - Control circuit power supply.

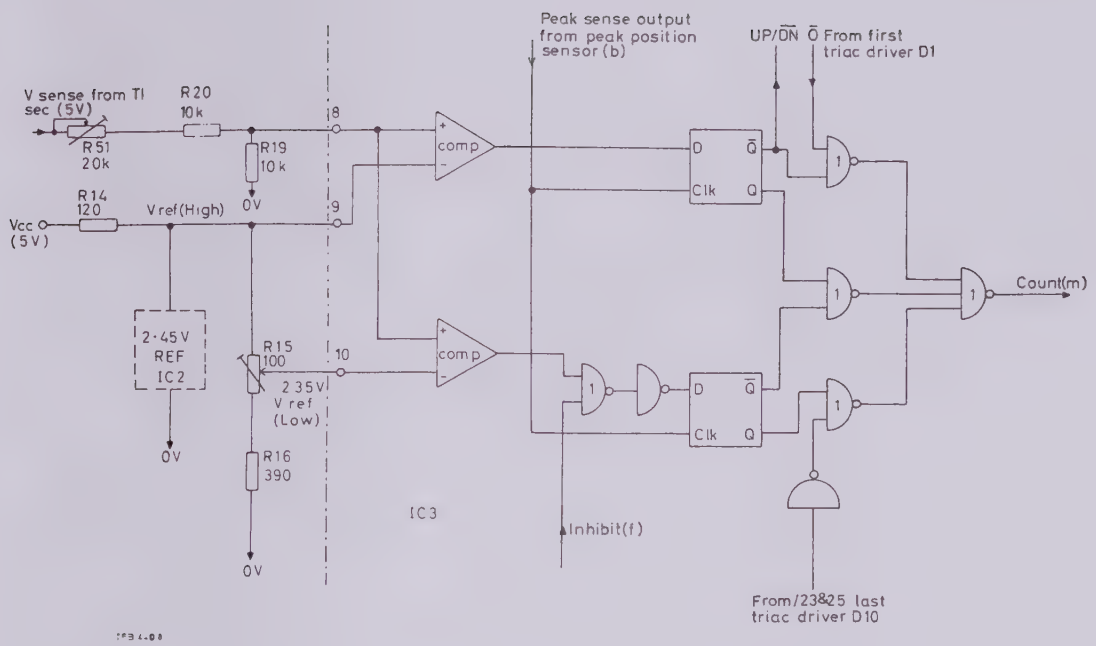


Fig. 53 Voltage sensor circuit (AP1)

Peak position sensor (AP1)

269. In this circuit an integrator consisting of R9, C7 and IC3 phase shifts the 3 V sine wave from T2 by 90° substituting a zero crossing for each peak. The comparator, part of IC3 takes the resulting waveform and compares it with the mean level on C2 to produce a square wave (IC3 pin 7) with its leading and trailing edges coincident with the peaks of the original sine wave. An inversion takes place in the comparator resulting in a negative edge coincident with the positive peak of the waveform and vice-versa.

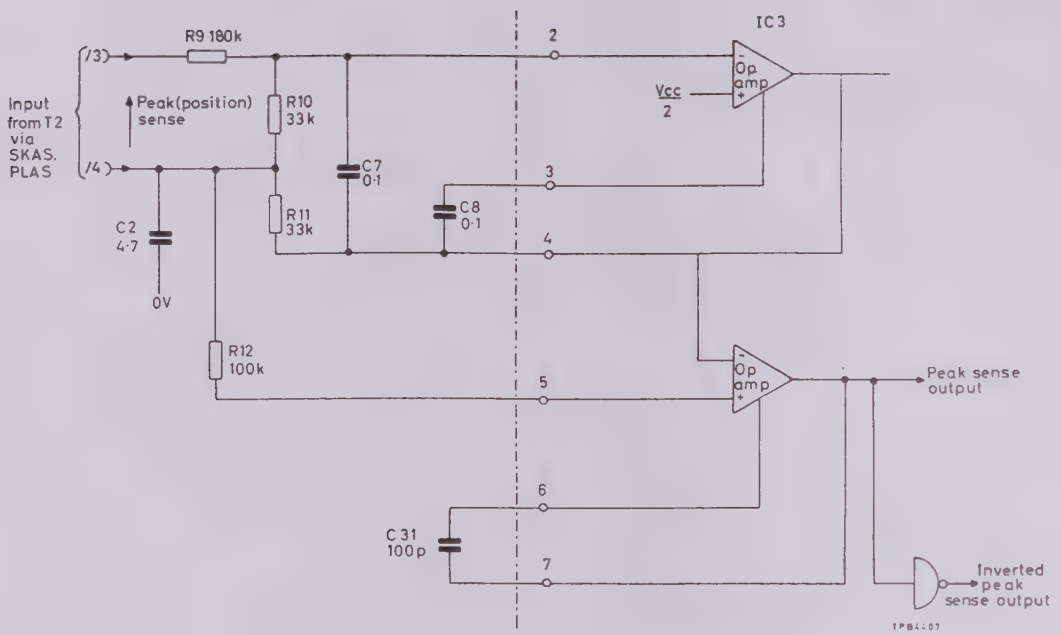


Fig. 54 Peak position sensor

Triac drivers (AP1)

270. One of the ten triac drivers is shown in Fig. 55 below. The Darlington pairs within IC4 and IC5 provide the required current and the transient protection networks, i.e. R21, R31 and C11 prevent spurious triggering.

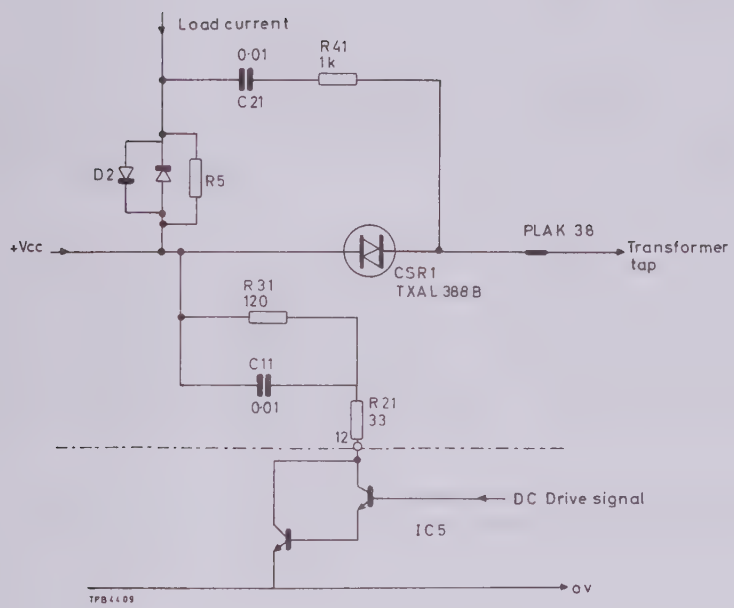


Fig. 55 Triac driver (AP1)

Voltage stabilizers (AP2)

271. Six separate regulated output voltages are provided; two of these, -12 V and +24 V, have fixed voltage outputs and three others, -5 V, +5 V and +12 V, are adjustable. All five regulators feature internal current limit and thermal shutdown, each has an l.e.d. indicator within the confines of the instrument to show the supply is on line.

272. The sixth regulator circuit gives a highly accurate low noise +70 V supply employing remote voltage sensing from unit AS5 via PLAN. Diodes D33, D34 and D35 provide the voltage offsets (from 70 V to 10 V) to operate TR1 series pass transistor. A connection from the +24 V supply line is also used to power IC4, a low noise feedback amplifier. TR2 with R19 is a current limiter protecting TR1 against momentary short circuits. TR3, R22 and R23 are supplied as a three part kit selected to give a standardized low noise reference, R15 sets the ripple null and R29, R30 are selected to give exactly +70 V output.

Keyboards (AK1, AK2, AK3)

Circuit diagram : Chap. 7, Fig. 4

273. Front panel selections are obtained using three separate printed circuit boards for convenience. The main keyboard, AK1, connects all the front panel keys to a six-by-six line matrix, this is fed via the latches board, AS2, to the microprocessor AL3. When a key is depressed both a vertical and a horizontal line are forced 'low', these are combined by the microprocessor to give a unique identification.

274. Keyboard AK2 includes two keys, UNLOCK/LOCK and COUNTER EXT; these are connected to the main AK1 matrix through plugs and sockets BK and AX. Also connected on this board are nine l.e.d's and a 4-10 line decoder providing an indication for eight of the nine selected frequency ranges. TR1 and D9 are connected direct to the input for the range 9 indication. Two further l.e.d's D10 and D11, are used to indicate REMOTE and ADDRESS modes and are lit by the microprocessor AL3 via the latches board, AS2.

275. Keyboard AK3 has five keys, all are connected through plugs and sockets PLBL and SKAX to the common matrix on board AK1.

Chapter 5

MAINTENANCE

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Annex
A Measurement of phase noise in signal generators

INTRODUCTION

1. This chapter contains information for keeping the equipment in good working order, checking overall performance, fault finding and realignment procedures. Before attempting any maintenance on the equipment you are advised to read the preceding chapter containing the technical description.

2. Test procedures described in this chapter may be simplified and of restricted range compared with those that relate to the generally more comprehensive factory test facilities, which are necessary to demonstrate complete compliance with the specifications.

3. Performance limits quoted are for guidance and should not be taken as guaranteed performance specifications unless they are also quoted in the performance data in Chap. 1. When making tests to verify that the instrument meets the stated performance limits, allowance must always be made for the uncertainty of the test equipment used.

4. In case of difficulties which cannot be resolved with the aid of this book, please contact our Service Division at the address given inside the rear cover, or your nearest Marconi Instruments representative. Always quote the type and serial number found on the data plate at the rear of the instrument.

5. Integrated circuit and semiconductor devices are used throughout this instrument and, although these have inherent long term reliability and mechanical ruggedness, they are susceptible to damage by overloading, reversed polarity and excessive heat or radiation and the use of insulation testers.

6. Numerous chip capacitors and resistors are fitted in this equipment. These have silver palladium end cap terminations. When soldering these device use solder containing 2% silver and a temperature controlled 45 watt soldering iron set to 315° (600°F). The use of a high wattage soldering iron will minimize the time taken to solder the device.

7. Static sensitive components. The c.m.o.s. integrated circuits used in this instrument have extremely high input resistance and can be damaged by accumulation of static charges. (See preliminary pages, Notes and Cautions.) Boards that have such integrated circuits all carry warning notices against damage by static discharge.

8. Beryllia health hazard. This material is used in the construction of some transistors in this equipment. These are transistors TR23 and TR26 on Unit AB2. Warning notices are displayed and extreme care must be exercised when wishing to disturb these. (See preliminary pages, Notes and Cautions.)

9. Bulkhead connectors and gaskets. Special care should be taken to ensure that no r.f. leakage occurs. To this end all bulkhead connectors and lid sealing gaskets should be secure. It is essential that the unit lids be correctly relocated in their slotted recesses after removal.

10. Fault location. Some aid to fault finding is provided by the typical d.c. voltage and signal levels. Tables given are not extensive but are intended as a pointer to further investigation. It is emphasized that each fault table should be studied having regard for the others, since incorrect operation of a circuit may be caused by malfunction of an associated circuit.

11. DC voltages. Voltages given approximate those which can be expected usi a 20 kΩ/V meter on a typical 2017 connected to an a.c. supply of 220 - 240 V, 50 Hz and unless stated otherwise were measured with the controls of the 2017 positioned as follows:-

CARRIER FREQUENCY	: 400 MHz
MODULATION OSCILLATOR	: ON, 1 kHz
AM DEPTH	: INT, 30%
FM DEVIATION	: INT
OUTPUT EMF	: +116 dB rel. 1 µV
FINE TUNE	: MID TRAVEL

12. Air cooling. Cooling of this instrument is effected by drawing cooling air through the filter at the rear of the instrument. The fan unit is mounted on the rear panel and requires no maintenance but the filter should be cleaned periodically.

(a) Withdraw the filter, first removing the cover from the rear panel.

(b) Clean the polyurethane foam of the filter with a suction cleaner and, if necessary, wash with hot soapy water. Under no circumstances should solvents be used.

(c) Shake the filter dry, if necessary, and replace.

ACCESS AND LAYOUT

Access (see Fig. 1)

13. Access to the instrument may be divided into four main areas : Logic Processor AL0, RF section AA0, RF section AB0 and the Master Oscillator, Gear box and Motor drive.

(i) The logic processor unit can be pivoted and secured in any one of three positions after first removing four conhex connectors and the air duct, see next para. for details.

Logic processor unit access. After further removing the lower logic processor unit cover, section AL4/AL5 can be hinged to expose the logic boards AL1-AL3.

(ii) The master oscillator and associated circuits are accessible when the logic processor unit has been placed in one of the three servicing positions.

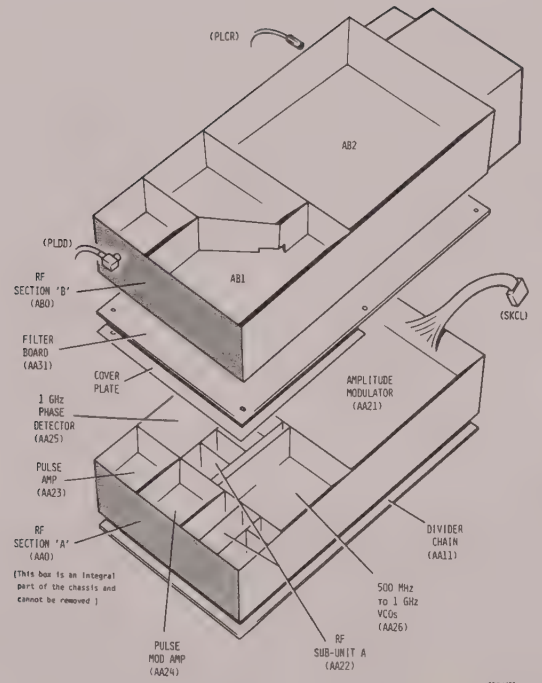
(iii) RF section AB0, boards AB1, AB2 and AB3 are also accessible when the logic processor unit is in the servicing position.

(iv) RF section AA0, boards AA21, AA22 and AA31 are accessed by removing the upper RF section AB0. Boards AA11, AS2, and the Attenuator AT1 are all accessible from underneath the instrument.

Logic processor unit (AL0) access

14. First remove the outside covers, both top and bottom are easily removed by withdrawing two fastening screws for each cover, these are secured to the rear panel.

(a) Remove the trim strips from the side of both front carrying handles, each of these are held by two countersunk screws.



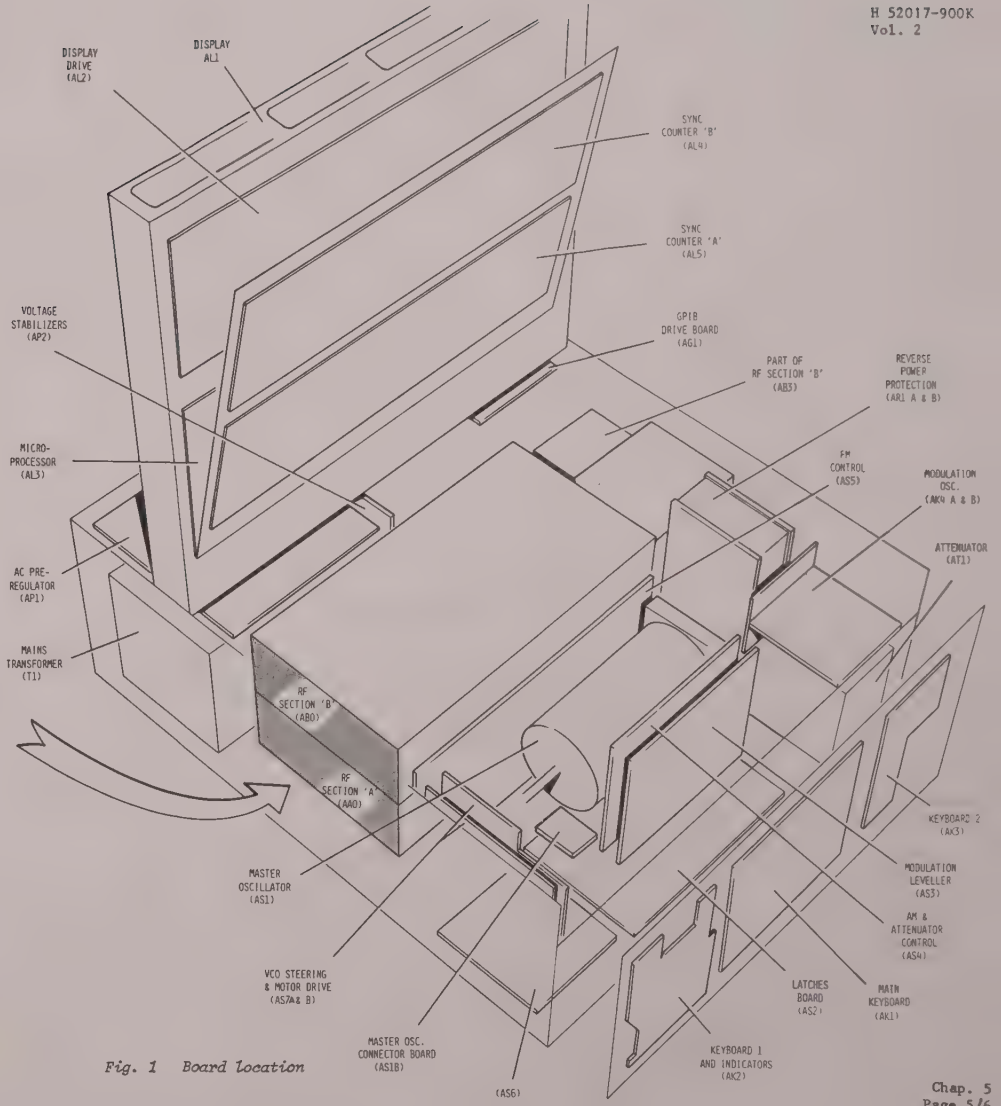


Fig. 1 Board location

(b) Remove the two front logic processor securing screws from the right-hand carrying handle - see Fig. 2 below - and similarly the corresponding screws on the left hand side carrying handle.

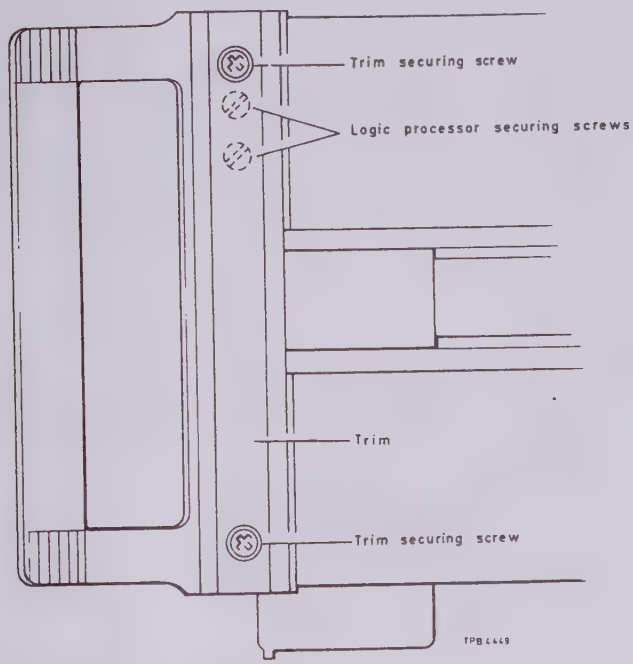


Fig. 2 Logic processor unit, front securing screws

(c) Detach the air duct from the rear of the logic processor unit shown in Fig. 3 below.

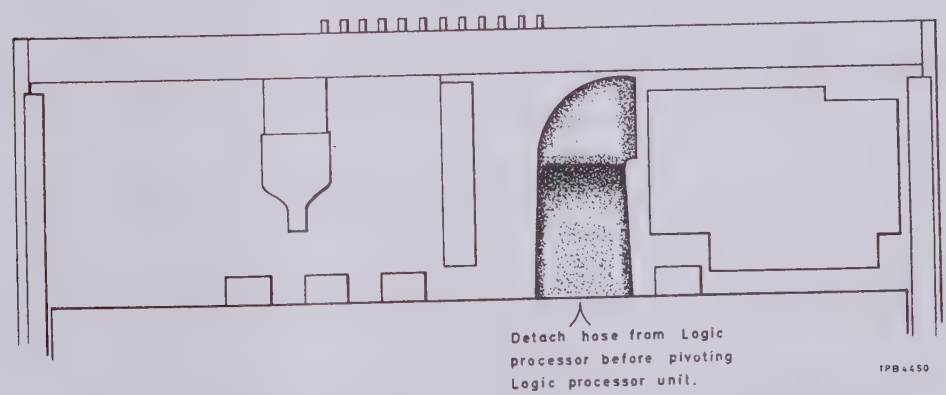


Fig. 3 Removal of air duct

(d) Before any attempt is made to pivot the logic processor unit it is essential that the four conhex plugs PLAU, PLAV, PLAW and PLDE are first disconnected. To ensure that this is not neglected a safety feature has been incorporated. A slide key plate is fitted in such a position that its tab protrudes through a keyhole in the side frame. This prevents the raising of the unit inadvertently. When the conhex plugs have been disconnected, the slide key plate can be moved sideways to release the tab from the side frame. The logic processor unit can then be pivoted into one of three positions and fixed using one of the two front securing screws as shown in Fig. 4 below.

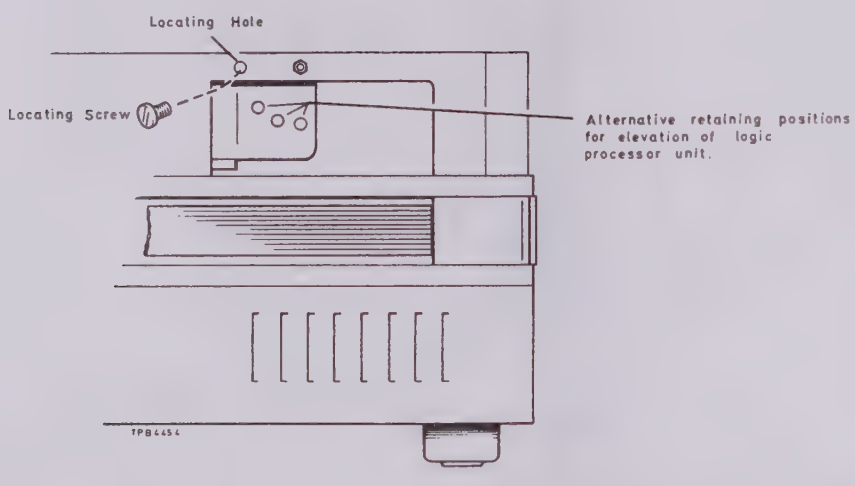


Fig. 4 Alternative fixing positions for logic processor unit

RF Section (AB0) removal

15. (a) Raise the logic processor unit and secure this in the vertical position.

(b) Remove AB0 lid held by four panhead screws, this will provide access to boards AB1 and AB2.

(c) Disconnect SKDU ribbon connector from unit AB3 situated on the side of box AB0.

(d) Remove the two semi-rigid conhex plugs PLCR (RF OUT) and PLDD (1 MHz IN) from the sides of the box AB0.

(e) Remove the four retaining screws securing the box to the lower RF Section AA0. Raise AB0 box slightly until the remining conhex plug PLCY interconnecting AB0 and AA0 is accessible under AB0. Disconnect this and also the air duct, then remove the box AB0.

⚠ On replacing AB0 box ensure that the air duct is refitted otherwise over heating and eventual damage will result.

RF Section (AA0) access

16. Access to board AA11 can be gained easily by removing the instrument's outside lower cover and also AA0 box lower lid. Board AA31 underside is visible when AB0 unit is removed, this is fastened by six panhead screws. Five of these hold in position spring contacts which must be replaced in the same position. Unless the spring contacts shown in Fig. 5 below are positioned correctly a risk of short circuits on the board is likely. When these are withdrawn AA31 can be raised to enable PLCJ and ribbon connector SKCL to be disconnected and the board removed. AA21 is then immediately accessible and AA23, AA24, AA25 when the cover plate held by six panhead screws is removed.

Fig. 5 Positioning of spring contacts (AA31)

Board layout and pre-set components

17. Printed circuit board component layouts can be seen in Chap. 7, Servicing diagrams, pre-set and select-in-calibration (SIC) components are also identified there. It is possible that some SICs such as C49, AB2 are only fitted to optimize, improve or set up a working parameter such as the HF response during initial manufacture and alignment. If the component is not in circuit no attempt should be made to fit it unless a relevant re-alignment procedure shows that its inclusion is necessary. Board location is shown in Fig. 1 and significant components on A0 chassis and rear panel are shown in Fig. 6 below.

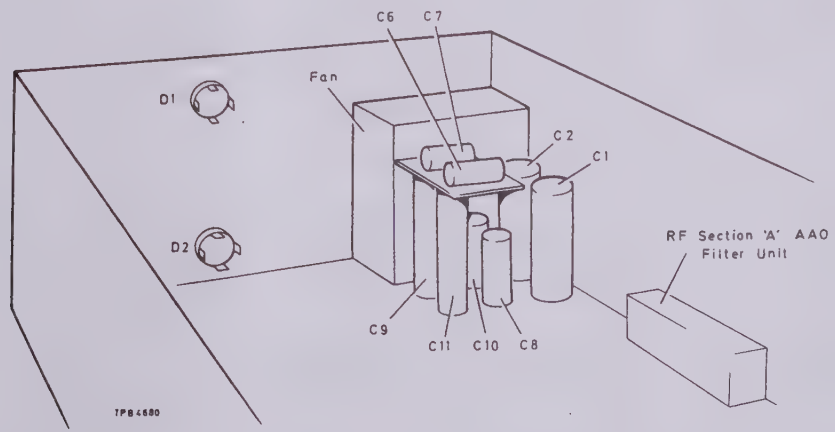


Fig. 6 Chassis components layout (A0)

Lamp replacement

18. The only front panel lamp fitted is the SUPPLY on indication (LP1). This may be removed by pulling firmly on the plastic lamp cover withdrawing the lamp and cover complete. The lamp can then be removed from the cover. To refit, replace the assembly by pressing firmly back into place.

PERFORMANCE CHECKS

Overall tests and adjustments

19. Many of the tests described in this chapter are simplified and of restricted range compared with those which would demonstrate compliance with the specification as described in paras. 1 to 4. If the results quoted in the following paragraphs are not obtainable refer to the related fault finding section and tables, and after repair ensure that realignment is carried out in accordance with that section, if applicable.

TABLE 1 TEST EQUIPMENT

Item	*Description*	*Minimum use specifications*	*Recommended model*
a	RF electronic millivoltmeter	Voltage range: 1mV to 3V r.m.s. Frequency range: 50kHz to 1024MHz Accuracy: ±5% of f.s.d. up to 50MHz ±2dB up to 900MHz ±3dB up to 1500MHz (using coaxial 'T' connector TM 7948)	TF 2603
b	T connector	VSWR ≤ 1.2:1 at 1500MHz, terminated in 50Ω.	TM 7948
c	N type 50Ω load	VSWR ≤ 1.05:1 up to 1500MHz.	TM 7967
d	Digital frequency meter	Frequency range: 10Hz to 2GHz. Sensitivity: 56mV r.m.s. p.d. into 50Ω. Input impedance: LF 1MHz in parallel with less than 25pF. Nominal 50Ω.	2435
e	Multimeter	Greater than 20kΩ/V.	GEC Selectest
f	Power meter	Power range measurement: 0.03μW to 3W. Accuracy: 1% of f.s.d. Frequency range: 10MHz to 1024MHz depending on the tft power head in use.	6460
g	Distortion factor meter	Fundamental range: 20Hz to 20kHz. Fundamental rejection: 80dB. Measurement accuracy: ±2% of full-scale ±2% of reading.	TF 2331A

TABLE 1 TEST EQUIPMENT (continued)

Item	*Description*	*Minimum use specifications*	*Recommended model*
h	AM/FM modulation meter	FM frequency range: 4 to 1024MHz Deviation range: 1.5 to 500kHz. AM frequency range: 4 to 400MHz. Modulation depth range: 30 & 100%. RF input frequency range: 4MHz to 1024MHz. Calibration accuracy: ±3%.	TF 2300B
i	AF oscillator	Frequency range: 10Hz to 110kHz Accuracy: ±3% of reading. Level: 0 to 3V. Distortion: Better than -100dB from 10Hz to 30kHz.	TF 2104
j	Digital voltmeter	DC volts. Ranges: ±200mV to ±1000V. Resolution: 0.1V on 1000V range (10µV on 200mV range). Accuracy: ±0.03% of reading +2 digits. DC current. Ranges: ±200 A - ±2000mA Resolution: ±0.01 A on lowest range 0.005% of range on all ranges. Accuracy: ±0.3% of reading +2 digits on all ranges.	
k	Psophometer		Hatfield Inst. type MBC1000 with A4/1000 fitted.
l	RF detector	Frequency range: 1MHz to 510MHz. Input impedance: Typically 10kΩ shunted by 2pF at 100MHz with an input of 0.5V r.m.s.	TM 9650/1
m	Spectrum analyser	Frequency range: 10kHz to 1.25GHz. Variable persistance/storage display.	
n	Probe unit	500Ω.	
o	AF voltmeter	Voltage range: 1mV to 100V f.s.d. Frequency range: 10Hz to 10MHz. Accuracy: ±1%.	TF 2600B
p	Oscilloscope with dual trace capability	Bandwidth: 50MHz. Sweep speeds: 1s/div. to 100ns/div.	TELEQUIPMENT D83 with S2C dual time-base unit.
q	Dual trace vertical amplifier	Deflection: 5mV to 20V/div. Accuracy: ±3%.	TELEQUIPMENT V4 dual trace amplifier
r	Differential amplifier	Bandwidth: 150kHz at 50µV/div. rising to 2MHz from 2mV/div. to 10V/div.	TELEQUIPMENT V3 differential amplifier.

TABLE 1 TEST EQUIPMENT (continued)

Item	*Description*	*Minimum use specifications*	*Recommended model*
s	Standard freq. source (1MHz)	Output level: 4V p-p. Frequency accuracy: 2 parts in 10^8.	Rubidium or Caesium reference unit.
t	Variable d.c. power supply	0 to 30V d.c. at 1A.	TF 2155/1
u	Sweep oscillator with RF plug-in unit	Frequency range: 5MHz to 1GHz. VSWR: ±0.1%.	6700B
v	Rho-bridge	Frequency range: 1MHz to 1GHz. Residual v.s.w.r.: ⟊ than 1.01:1 from 5MHz to 1GHz, ⟊ than 1.03:1 below 5MHz. Characteristic impedance: 50Ω.	
	Standard and calibrated mismatched loads	55Ω, 1.1:1; 60Ω, 1.2:1; 70Ω, 1.4:1.	
w	Logic probe		
x	Bus fault analyser		ICS ELECTRONICS CORPORATION Model 4810
y	GPIB lead assy.		43129-189U

TABLE 2 DECIBEL CONVERSION TABLE

Ratio Down			Ratio Up	
VOLTAGE	POWER	DECIBELS	VOLTAGE	POWER
1·0	1·0	0	1·0	1·0
·9886	·9772	·1	1·012	1·023
·9772	·9550	·2	1·023	1·047
·9661	·9333	·3	1·035	1·072
·9550	·9120	·4	1·047	1·096
·9441	·8913	·5	1·059	1·122
·9333	·8710	·6	1·072	1·148
·9226	·8511	·7	1·084	1·175
·9120	·8318	·8	1·096	1·202
·9016	·8128	·9	1·109	1·230
·8913	·7943	1·0	1·122	1·259
·8710	·7586	1·2	1·148	1·318
·8511	·7244	1·4	1·175	1·380
·8318	·6918	1·6	1·202	1·445
·8128	·6607	1·8	1·230	1·514
·7943	·6310	2·0	1·259	1·585
·7762	·6026	2·2	1·288	1·660
·7586	·5754	2·4	1·318	1·738
·7413	·5495	2·6	1·349	1·820
·7244	·5248	2·8	1·380	1·905
·7079	·5012	3·0	1·413	1·995
·6683	·4467	3·5	1·496	2·239
·6310	·3981	4·0	1·585	2·512
·5957	·3548	4·5	1·679	2·818
·5623	·3162	5·0	1·778	3·162
·5309	·2818	5·5	1·884	3·548
·5012	·2512	6	1·995	3·981
·4467	·1995	7	2·239	5·012
·3981	·1585	8	2·512	6·310
·3548	·1259	9	2·818	7·943
·3162	·1000	10	3·162	10·000
·2818	·07943	11	3·548	12·59
·2512	·06310	12	3·981	15·85
·2239	·05012	13	4·467	19·95
·1995	·03981	14	5·012	25·12
·1778	·03162	15	5·623	31·62

TABLE 2 DECIBEL CONVERSION TABLE (continued)

Ratio Down			Ratio Up	
VOLTAGE	POWER	DECIBELS	VOLTAGE	POWER
·1585	·02512	**16**	6·310	39·81
·1413	·01995	**17**	7·079	50·12
·1259	·01585	**18**	7·943	63·10
·1122	·01259	**19**	8·913	79·43
·1000	·01000	**20**	10·000	100·00
·07943	$6{\cdot}310 \times 10^{-3}$	**22**	12 59	158·5
·06310	$3{\cdot}981 \times 10^{-3}$	**24**	15·85	251·2
·05012	$2{\cdot}512 \times 10^{-3}$	**26**	19·95	398·1
·03981	$1{\cdot}585 \times 10^{-3}$	**28**	25 12	631 0
·03162	$1{\cdot}000 \times 10^{-3}$	**30**	31·62	1,000
·02512	$6{\cdot}310 \times 10^{-4}$	**32**	39·81	$1{\cdot}585 \times 10^{3}$
·01995	$3{\cdot}981 \times 10^{-4}$	**34**	50·12	$2{\cdot}512 \times 10^{3}$
·01585	$2{\cdot}512 \times 10^{-4}$	**36**	63·10	$3{\cdot}981 \times 10^{3}$
·01259	$1\ 585 \times 10^{-4}$	**38**	79·43	$6{\cdot}310 \times 10^{3}$
·01000	$1{\cdot}000 \times 10^{-4}$	**40**	100·00	$1{\cdot}000 \times 10^{4}$
$7{\cdot}943 \times 10^{-3}$	$6{\cdot}310 \times 10^{-5}$	**42**	125·9	$1{\cdot}585 \times 10^{4}$
$6{\cdot}310 \times 10^{-3}$	$3\ 981 \times 10^{-5}$	**44**	158·5	$2\ 512 \times 10^{4}$
$5{\cdot}012 \times 10^{-3}$	$2{\cdot}512 \times 10^{-5}$	**46**	199·5	$3{\cdot}981 \times 10^{4}$
$3\ 981 \times 10^{-3}$	$1{\cdot}585 \times 10^{-5}$	**48**	251·2	$6{\cdot}310 \times 10^{4}$
$3{\cdot}162 \times 10^{-3}$	$1{\cdot}000 \times 10^{-5}$	**50**	316·2	$1{\cdot}000 \times 10^{5}$
$2{\cdot}512 \times 10^{-3}$	$6{\cdot}310 \times 10^{-6}$	**52**	398·1	$1{\cdot}585 \times 10^{5}$
$1{\cdot}995 \times 10^{-3}$	$3{\cdot}981 \times 10^{-6}$	**54**	501·2	$2{\cdot}512 \times 10^{5}$
$1{\cdot}585 \times 10^{-3}$	$2{\cdot}512 \times 10^{-6}$	**56**	631·0	$3{\cdot}981 \times 10^{5}$
$1{\cdot}259 \times 10^{-3}$	$1{\cdot}585 \times 10^{-6}$	**58**	794·3	$6{\cdot}310 \times 10^{5}$
$1{\cdot}000 \times 10^{-3}$	$1{\cdot}000 \times 10^{-6}$	**60**	1,000	$1{\cdot}000 \times 10^{6}$
$5{\cdot}623 \times 10^{-4}$	$3{\cdot}162 \times 10^{-7}$	**65**	$1{\cdot}778 \times 10^{3}$	$3{\cdot}162 \times 10^{6}$
$3{\cdot}162 \times 10^{-4}$	$1\ 000 \times 10^{-7}$	**70**	$3{\cdot}162 \times 10^{3}$	$1{\cdot}000 \times 10^{7}$
$1{\cdot}778 \times 10^{-4}$	$3{\cdot}162 \times 10^{-8}$	**75**	$5{\cdot}623 \times 10^{3}$	$3{\cdot}162 \times 10^{7}$
$1{\cdot}000 \times 10^{-4}$	$1{\cdot}000 \times 10^{-8}$	**80**	$1{\cdot}000 \times 10^{4}$	$1{\cdot}000 \times 10^{8}$
$5{\cdot}623 \times 10^{-5}$	$3{\cdot}162 \times 10^{-9}$	**85**	$1{\cdot}778 \times 10^{4}$	$3{\cdot}162 \times 10^{8}$
$3{\cdot}162 \times 10^{-5}$	$1{\cdot}000 \times 10^{-9}$	**90**	$3{\cdot}162 \times 10^{4}$	$1{\cdot}000 \times 10^{9}$
$1{\cdot}000 \times 10^{-5}$	$1{\cdot}000 \times 10^{-10}$	**100**	$1{\cdot}000 \times 10^{5}$	$1{\cdot}000 \times 10^{10}$
$3{\cdot}162 \times 10^{-6}$	$1{\cdot}000 \times 10^{-11}$	**110**	$3{\cdot}162 \times 10^{5}$	$1{\cdot}000 \times 10^{11}$
$1{\cdot}000 \times 10^{-6}$	$1{\cdot}000 \times 10^{-12}$	**120**	$1{\cdot}000 \times 10^{6}$	$1{\cdot}000 \times 10^{12}$
$3{\cdot}162 \times 10^{-7}$	$1{\cdot}000 \times 10^{-13}$	**130**	$3\ 162 \times 10^{6}$	$1{\cdot}000 \times 10^{13}$
$1{\cdot}000 \times 10^{-7}$	$1{\cdot}000 \times 10^{-14}$	**140**	$1{\cdot}000 \times 10^{7}$	$1{\cdot}000 \times 10^{14}$

TABLE 3 dBμV CONVERSION TABLE

dBm	EMF (r.m.s.)	dBμV (e.m.f.)	dBm	EMF (r.m.s.)	dBμV (e.m.f.)	dBm	EMF (r.m.s.)	dBμV (e.m.f.)
-130	.141μV	-17	-80	44.7μV	+33	-30	14.1mV	+83
-129	.159	-16	-79	50.2	+34	-29	15.9	+84
-128	.178	-15	-78	56.3	+35	-28	17.8	+85
-127	.200	-14	-77	63.2	+36	-27	20.0	+86
-126	.224	-13	-76	70.9	+37	-26	22.4	+87
-125	.251	-12	-75	79.5	+38	-25	25.1	+88
-124	.282	-11	-74	89.2	+39	-24	28.2	+89
-123	.317	-10	-73	100	+40	-23	31.7	+90
-122	.355	-9	-72	112	+41	-22	35.5	+91
-121	.399	-8	-71	126	+42	-21	39.9	+92
-120	.447	-7	-70	141	+43	-20	44.7	+93
-119	.502	-6	-69	159	+44	-19	50.2	+94
-118	.563	-5	-68	178	+45	-18	56.3	+95
-117	.632	-4	-67	200	+46	-17	63.2	+96
-116	.700	-3	-66	224	+47	-16	70.9	+97
-115	.795	-2	-65	251	+48	-15	79.5	+98
-114	.892	-1	-64	282	+49	-14	89.2	+99
-113	1.00	0	-63	317	+50	-13	100	+100
-112	1.12	+1	-62	355	+51	-12	112	+101
-111	1.20	+2	-61	399	+52	-11	126	+102
-110	1.41	+3	-60	447	+53	-10	141	+103
-109	1.59	+4	-59	502	+54	-9	159	+104
-108	1.78	+5	-58	563	+55	-8	178	+105
-107	2.00	+6	-57	632	+56	-7	200	+106
-106	2.24	+7	-56	709	+57	-6	224	+107
-105	2.51	+8	-55	795	+58	-5	251	+108
-104	2.82	+9	-54	892	+59	-4	282	+109
-103	3.17	+10	-53	1.00mV	+60	-3	317	+110
-102	3.55	+11	-52	1.12	+61	-2	355	+111
-101	3.99	+12	-51	1.26	+62	-1	399	+112
-100	4.47	+13	-50	1.41	+63	0	447	+113
-99	5.02	+14	-49	1.59	+64	+1	502	+114
-98	5.63	+15	-48	1.78	+65	+2	563	+115
-97	6.32	+16	-47	2.00	+66	+3	632	+116
-96	7.09	+17	-46	2.24	+67	+4	709	+117
-95	7.95	+18	-45	2.51	+68	+5	795	+118
-94	8.92	+19	-44	2.82	+69	+6	892	+119
-93	10.0	+20	-43	3.17	+70	+7	1.00V	+120
-92	11.2	+21	-42	3.55	+71	+8	1.12	+121
-91	12.6	+22	-41	3.99	+72	+9	1.26	+122
-90	14.1	+23	-40	4.47	+73	+10	1.41	+123
-89	15.9	+24	-39	5.02	+74	+11	1.59	+124
-88	17.8	+25	-38	5.63	+75	+12	1.78	+125
-87	20.0	+26	-37	6.32	+76	+13	2.00	+126
-86	22.4	+27	-36	7.09	+77	+14	2.24	+127
-85	25.1	+28	-35	7.95	+78	+15	2.51	+128
-84	28.2	+29	-34	8.92	+79	+16	2.82	+129
-83	31.7	+30	-33	10.0	+80	+17	3.17	+130
-82	35.5	+31	-32	11.2	+81	+18	3.55	+131
-81	39.9	+32	-31	12.6	+82	+19	3.99	+132
						+20	4.47	+133

RF output

Test equipment : items a, RF electronic millivoltmeter
b, T connector
c, N type 50 Ω load
f, Power meter

20. The following check verifies the action of the a.l.c. at the a.m. maximum output.

(1) Set the MODULATION OSCILLATOR, AM and FM MODULATION switches to OFF.

(2) Enter an RF LEVEL of +13 dBm (2 V e.m.f.).

(3) Connect the millivoltmeter to the output of the signal generator see Fig. 7 below. Set the millivoltmeter to its highest range.

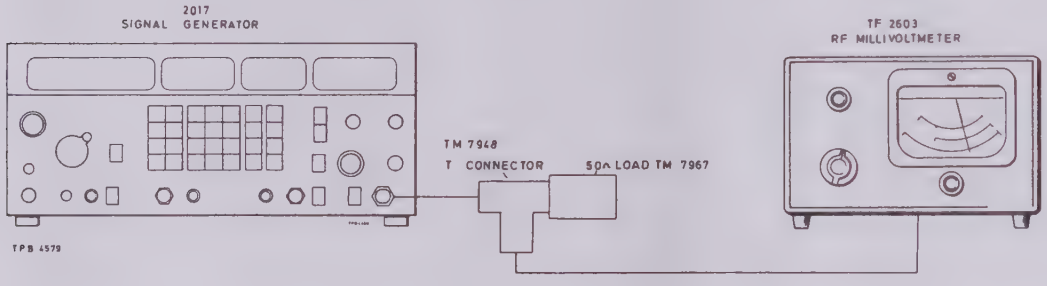


Fig. 7 Test gear arrangement for r.f. output measurements

(4) Switch ON the RF OUTPUT and observe a reading of approximately 1 V p.d. (2 V e.m.f.).

(5) Make random selections throughout the frequency range of the instrument and observe that the output level remains constant within ±1 dB for frequencies up to 512 MHz and within ±2 dB for frequencies between 512 and 1024 MHz. When checking carrier frequencies above 50 MHz it is recommended that a power meter be used with the appropriate tft power head.

(6) Set FM and AM MODULATION OFF and enter an RF LEVEL of +19 dBm (4 V e.m.f.). Check that the maximum r.f. output level (f.m. and c.w. mode only) remains constant as in step (5) above.

Coarse attenuator functional check

Test equipment : items m, Spectrum analyser
n, Probe unit 1GHz/500 Ω

21. Each of the coarse attenuator relays and pads can be checked by connecting the spectrum analyser to the 2017 RF OUTPUT socket. Select CARRIER FREQ of 100 MHz and tune the spectrum analyser to this signal. Select in turn each of the r.f. levels given in Table 4 below to confirm that the correct logic is being applied and that as each relay functions the nominal value of attenuation is obtained. Confirmation that continuity exists through all the relay contacts both in the energized and de-energized conditions is also obtained.

TABLE 4 ATO ATTENUATOR FUNCTIONAL CHECK

Selected r.f. level	*Relay state*	*Pads in circuit*
+7dBm	All relays energized	No pads in circuit
+1dBm	RLE de-energized	No.5 (6dB)
-5dBm	RLC de-energized	No.3 (12dB)
-17dBm	RLF de-energized	No.6 (24dB)
-29dBm	RLD,RLE de-energized	No.4,5 (30dB,6dB)
-59dBm	RLA,RLB,RLE de-energized	No.1,2,5 (30dB,30dB,6dB)

22. The only electrical adjustment provided on AT1 board is a series of flags which are used to adjust the calibration of each pad at 1 GHz. To carry out comprehensive attenuator accuracy checks and re-alignment requires each pad to be separately set up using specialized measuring facilities and it is recommended that this be carried out only by the nearest Marconi Instruments agent or Service Division.

Frequency accuracy

Test equipment : items d, Digital frequency meter
s, Standard frequency source (1 MHz)

23. (1) Connect the frequency meter to the output of the instrument.

(2) It is advisable to synchronize the frequency meter with an external standard frequency accuracy 2 parts in 10^8 if possible.

(3) With the 2017 in any mode of operation and the INT/EXT STD switch set to INT STD OUT carry out spot checks throughout the range of the instrument and ensure that frequencies are within the specifications.

(4) Check that the INT STD OUT socket provides the correct output, a 4 V p-p t.t.l. frequency signal at 1 MHz ±0.1 Hz.

Modulation oscillator performance

Test equipment : items d, Digital frequency meter
g, Distortion factor meter

24. To check the frequency, distortion and output of the modulation oscillator proceed as follows:-

(1) Connect the counter to the modulation output socket, OUT 600 Ω (output level is 1 V e.m.f. ±20% at 600 Ω).

(2) Switch the MODULATION OSCILLATOR in turn to both 400 Hz and 1 kHz fixed frequencies and check that the indicated counter frequency corresponds to the one selected ±5%.

(3) Disconnect the counter and connect the distortion factor meter to the OUT 600 Ω socket. Select any audio frequency and check that the measured distortion does not exceed 0.5%.

(4) Switch the distortion factor meter to the Hi Z and check that the output level is 2 V r.m.s. ±20%.

FM deviation

Test equipment : item h, AM/FM modulation meter

25. To check the deviation accuracy proceed as follows:-

(1) Select CARRIER FREQ to any frequency within Ranges 3 to 9 (Ranges 1 and 2 are limited to a maximum of 40 kHz deviation). Set FM DEVIATION to 75 kHz, INT, MODULATION OSCILLATOR to 1 kHz, FM MODULATION ON.

(2) Connect the modulation meter to the RF OUTPUT socket and tune to the carrier frequency. Measure the deviation and check that it is within 4% of the deviation selected +50 Hz.

FM tracking

Test equipment : item h, AM/FM modulation meter

26. To check the f.m. tracking proceed as follows:-

(1) Connect the modulation meter to the 2017 RF OUTPUT socket.

(2) Set FM DEVIATION to 160 kHz, INT, MODULATION OSCILLATOR to 1 kHz, FM MODULATION ON.

(3) Select the CARRIER FREQ to various frequencies between 16.1 and 32 MHz and tune the modulation meter to the same. Check that the output deviation remains at 160 kHz ±4% +50 Hz.

AM depth

Test equipment : item h, AM/FM modulation meter

27. To check the a.m. depth proceed as follows:-

(1) Connect the modulation meter to the RF OUTPUT socket.

(2) Select CARRIER FREQ to any frequency up to 400 MHz, AM DEPTH to 80%, INT, MODULATION OSCILLATOR to 1 kHz, AM MODULATION ON.

(3) Tune the modulation meter to the carrier frequency of the 2017. Check the AM depth and ensure the accuracy is better than ±3% depth up to 80% for carrier frequencies up to 400 MHz.

28. If a modulation meter is not available the a.m. depth can be assessed by using an oscilloscope to measure the peak and trough values of the modulation envelope. The a.m. depth is then determined by

$$\text{AM depth } \% = \frac{Vp - Vt}{Vp + Vt} \times 100$$

Where Vp and Vt are the measured peak-to-peak and trough-to-trough amplitudes respectively.

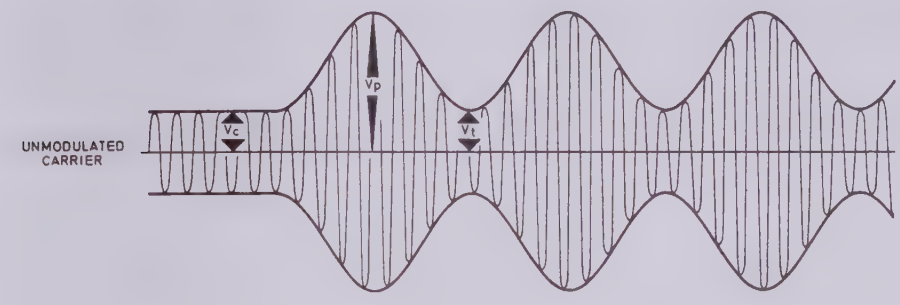


Fig. 8 Modulation depth measurement

External a.m. modulation frequency and level range

Test equipment : items h, AM/FM modulation meter
i, AF oscillator
o, AF voltmeter

29. The modulation depth should remain constant for audio levels of between 0.5 and 1.5 V into 600 Ω, and frequencies between 20 Hz to 50 kHz. This sensitivity can be checked as follows:-

(1) Connect the test equipment as shown in Fig. 9 below.

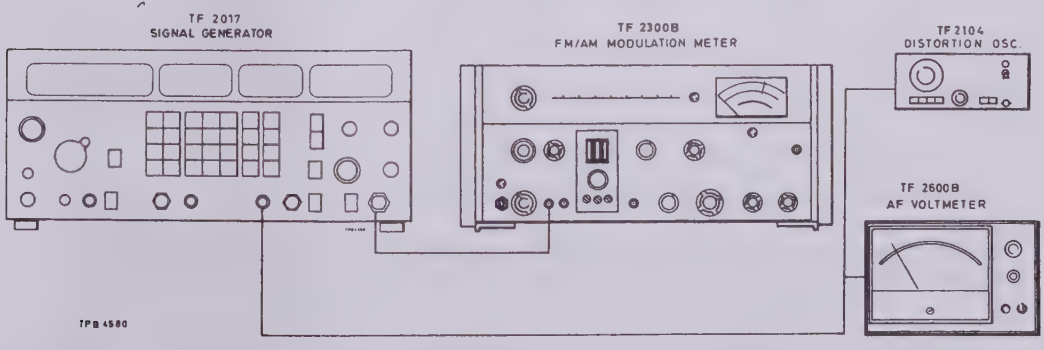


Fig. 9 Test gear arrangement for the checking of external modulation sensitivity

(2) Select CARRIER FREQ 100 MHz, AM DEPTH 80% EXT, LEVELLED, RF LEVEL 0 dBm, tune the modulation meter to the carrier frequency.

(3) Select 1 kHz on the oscillator unit and adjust the output level for a reading of 1 V on the AF voltmeter. Check that the modulation reading is 80% ±3% and that the 2017 AM DEPTH OFF annunciator is not flashing.

(4) Ensure that the modulation reading is maintained and that the AM DEPTH OFF annunciator remains unlit between inputs of 0.5 - 1.5 V.

(5) Further select other audio frequencies on the oscillator unit within the range 20 Hz to 50 kHz maintaining the output level of 1 V and check that the modulation reading is maintained at 80% ±3%.

AM distortion

Test equipment : items g, Distortion factor meter
h, AM/FM modulation meter

30. To check the internal a.m. distortion proceed as follows:-

(1) Connect the test equipment as shown in Fig. 10 below.

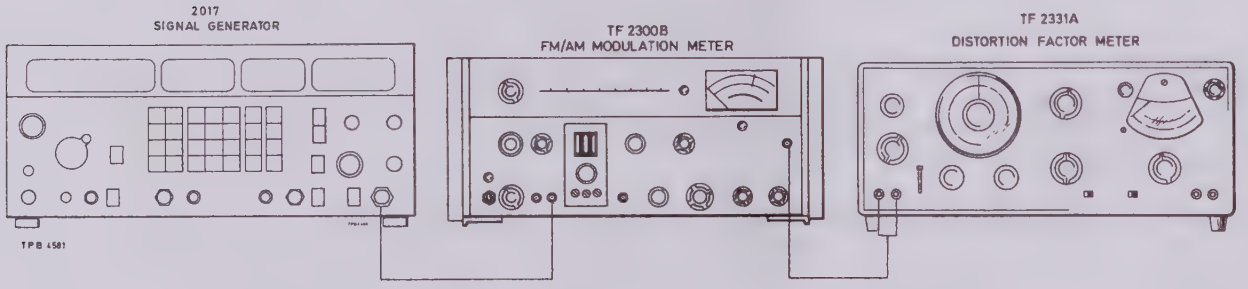


Fig. 10 Test gear arrangement for checking f.m. and a.m. distortion and f.m. on c.w.

(2) Select CARRIER FREQ 100 MHz, AM DEPTH 80% INT, MODULATION OSCILLATOR 1 kHz. Tune the modulation meter to the 100 MHz signal, check that the total harmonic distortion is less than 3.5%.

(3) Select AM DEPTH of 30% and check that the total harmonic distortion is less than 3.0%. Select further carrier frequencies up to 400 MHz and check that the total harmonic distortion figure is not exceeded.

FM distortion

Test equipment : items g, Distortion factor meter
h, AM/FM modulation meter

31. To check the f.m. distortion proceed as follows:-

(1) Connect the test equipment as shown in Fig. 10. Select CARRIER FREQ 20 MHz, MODULATION OSCILLATOR 1 kHz, FM DEVIATION 160 kHz INT, RF OUTPUT LEVEL 0 dBm.

(2) Tune the modulation meter to the instrument and check that the distortion is not in excess of 2% t.h.d. Repeat the test with lower amounts of deviation.

Spurious f.m. on c.w.

Test equipment : items g, Distortion factor meter
h, AM/FM modulation meter

32. The unwanted spurious f.m. components on this instrument are of a very low order, less than 5 Hz. Test equipment necessary to check this is of a specialized nature and would not normally be available in general use. Users can however determine whether the spurious f.m. is excessive using FM Modulation Meter TF 2300B and the Distortion Factor Meter TF 2331A.

Spurious a.m. on c.w.

Test equipment : items k, Psophometer
l, RF detector

33. To check the unwanted a.m. on c.w. output proceed as follows:-

(1) Connect the test equipment as shown below in Fig. 11.

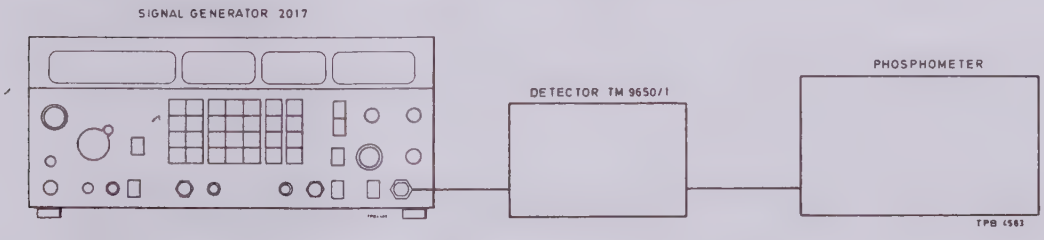


Fig. 11 Test gear arrangement for checking spurious a.m. on c.w.

(2) Select CARRIER FREQ 100 MHz; MODULATION OSCILLATOR 1 kHz, AM DEPTH 30% INT, RF LEVEL +12.9 dBm.

(3) The psophometer controls should be set as follows:-

INPUT SELECTOR	:	THRO
WEIGHTING	:	FILTER No. 1
VOLTAGE/dBm	:	to suit detector output

(4) Switch the psophometer to INTERNAL SUPPLY. Adjust the VOLTAGE/dBm range switch and CALIBRATION control for a convenient indication on the meter. Note the VOLTAGE/dBm range setting and the meter reading.

(5) Switch AM MODULATION OFF and MODULATION OSCILLATOR OFF. Increase the VOLTAGE/dBm range setting by 54 dB. The meter should indicate a level which is below that noted in step (4).

VSWR (5 MHz to 1 GHz)

Test equipment : items p,q, Oscilloscope with dual trace capability
u, Sweep oscillator with r.f. plug-in unit
v, Rho-bridge with standard loads and calibrated mismatch

34. The impedance measurement may be carried out over almost all the frequency range of the instrument. Connect the test equipment as shown in Fig. 12 below.

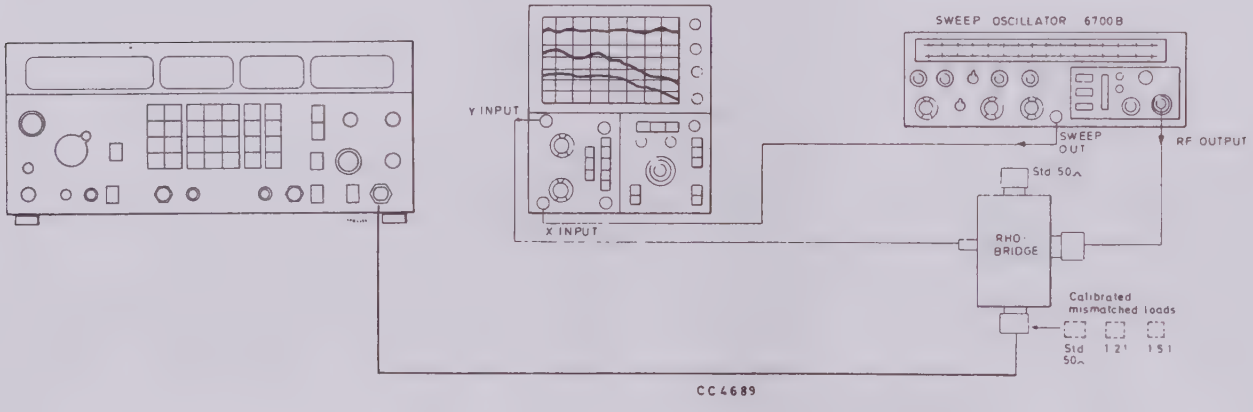


Fig. 12 Test gear arrangement for checking v.s.w.r.

(1) Set the sweep oscillator to F1-F2 and sweep from 5 MHz to 1 GHz, insert standard 50 Ω loads into the rho-bridge and set datum point near the top of the oscilloscope display. Replace one 50 Ω with a 1.1:1 mismatched load and adjust the d.c. output of the rho-bridge so that the vertical deflection of the oscilloscope occupies 3 or 4 c.m.s. for the mismatch change. Using a chinagraph draw the pattern on the oscilloscope graticule.

(2) Remove the 1.1:1 mismatched load and connect the 1.2:1 load drawing a further pattern on the oscilloscope graticule, repeat the operation with the 1.4:1 load.

(3) Remove the 1.4:1 mismatched load and connect the 2017 to the rho-bridge instead, check that the v.s.w.r. indicated on the oscilloscope does not exceed 1.15:1 up to 256 MHz, 1.25:1 up to 512 MHz and 1.35:1 up to 1 GHz. The RF LEVEL of the 2017 should be set to below 0 dBm.

Carrier harmonics and spurious signals

Test equipment : items m, Spectrum analyser
n, Probe unit 1 GHz/500 Ω

35. Carrier harmonics. To check the level of harmonics of the carrier frequency in a c.w. output proceed as follows:-

(1) Connect the spectrum analyser to the RF OUTPUT socket and set the instrument to give a c.w. output at a convenient level below +13 dBm.

(2) Tune the instrument through its r.f. range and check that harmonics are better than -27 dBc.

(3) Check that for carrier frequencies above 512 MHz any sub-harmonics generated are better than -70 dBs. Carrier frequencies between 4 - 512 MHz generate no sub-harmonics.

36. Non-harmonic components. Check that for carrier frequencies between 10 kHz - 4 MHz non-harmonic components are better than -50 dBc. None are generated between 4 - 1024 MHz.

Reverse power protection (RPP)

Test equipment : items e, Multimeter
t, Variable d.c. power supply

37. Set the d.c. power supply to +5 V and apply this to the 2017 RF OUTPUT 50 Ω socket causing the RPP circuit to trip.

(1) An indication that the reverse power limit has been exceeded is given by the RF OFF annunciator which will give either a flashing indication, or if the d.c. is still applied, a steady on state (for details see REVERSE POWER PROTECTION Vol. 1, Chap. 3).

(2) Remove the +5 V source and check that no continuity exists between the 'N' type connector centre pin and earth (taking care not to damage the connector pin).

(3) Reset the RPP by pressing the RF ON/OFF key and ensure that the RF OFF annunciator turns off. Set the d.c. power supply to -5 V and apply this again to the RF OUTPUT 50 Ω socket checking that the RPP again trips. Remove the d.c. source and reset the RPP.

FAULT LOCATION

38. The following section consists of fault finding charts and tests to aid fault diagnosis as follows:-

(1) Start with the general fault finding chart, Table 5, which will help to localize the area. The table will either indicate the area of the fault or indicate to a further table or relevant paragraph in this chapter.

(2) To assist fault finding it is advisable to study the appropriate part of the description in Chap. 4. When a fault is localized to a p.c.b. check that the input supply voltages to that board are present. Before carrying out any soldering read the precautions regarding chip components in para. 6 of this chapter.

(3) Plug and socket pin numbers are, where possible, identified by placing pin number 1 on the p.c.b. legend. Each pin thereafter follows the normal convention for numbering integrated circuits.

Voltage checks

39. Remove both outer instrument covers.

(1) Locate board AP2 and check that all five l.e.d's connected to the following supplies are lit, +5 V, +12 V, +24 V, -12 V and -5 V. To measure these voltages, locate the RF Section 'A' filter box. This is situated on the right-hand side of the instrument. Identify the feed through capacitors shown in Fig. 13 below and connect the d.v.m. between the relevant capacitor and earth. Each supply should be accurate to within 10%.

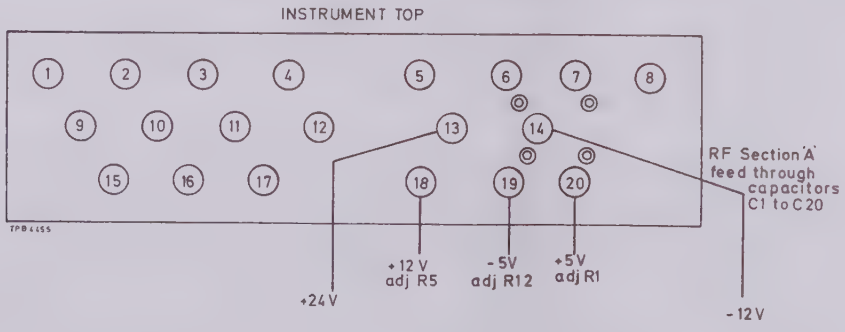


Fig. 13 Measurement of stabilized voltages AP2

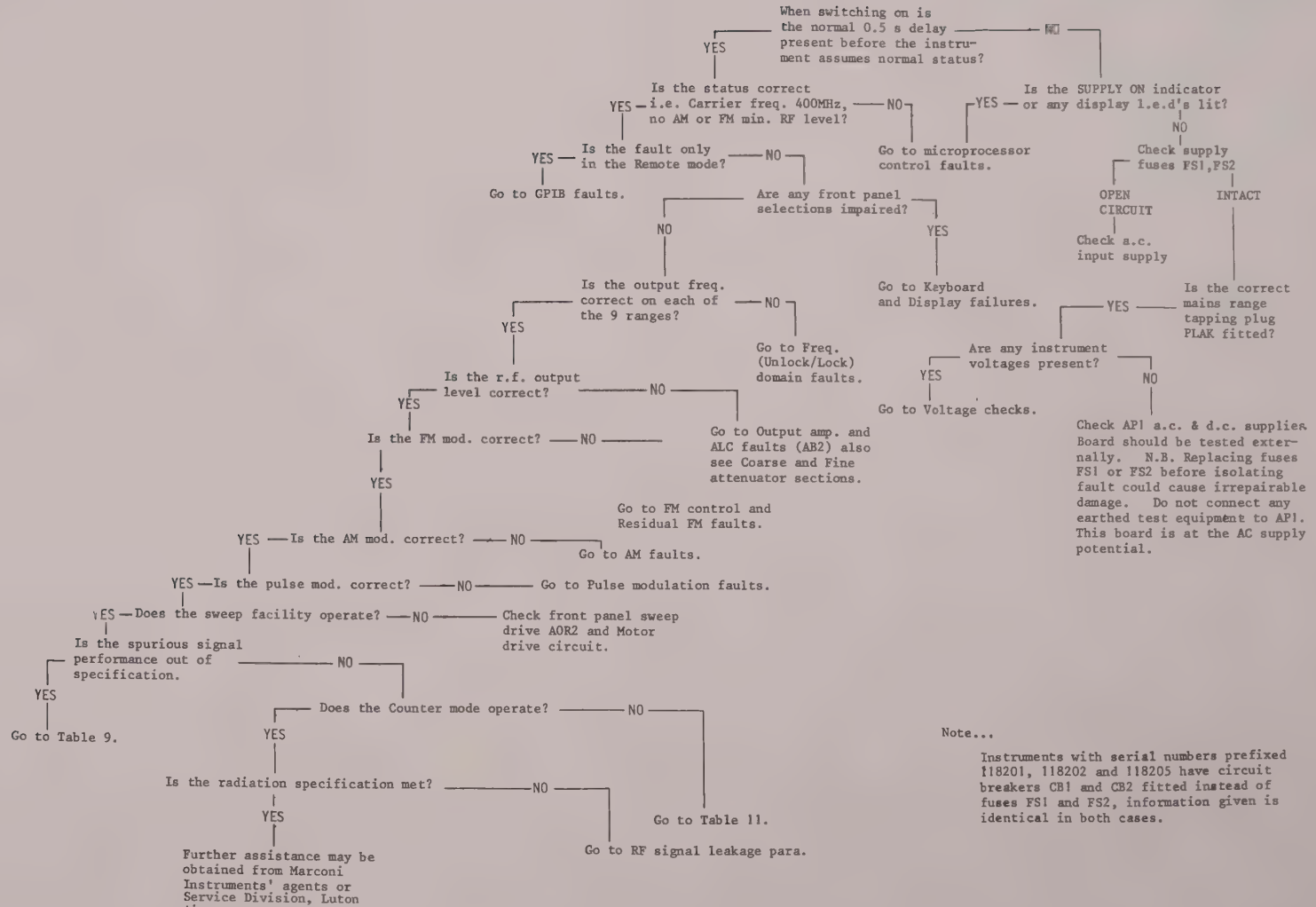


TABLE 5 GENERAL FAULT FINDING CHART

Note...

Instruments with serial numbers prefixed 118201, 118202 and 118205 have circuit breakers CB1 and CB2 fitted instead of fuses FS1 and FS2, information given is identical in both cases.

(2) Check that the +70 V low noise supply reads +70.5 V ±0.5 V by connecting the d.v.m. negative terminal to the collector outside cannister of TR2 (this can be identified by reference to the component layout of board AP2 Chap. 7, Fig. 5a). The voltage at this point will be 0.5 V higher than the actual reference level but allows the measurement to be taken without raising the logic processor unit or withdrawing AP2 board from the instrument.

(3) To adjust any of the above voltages it is necessary to withdraw AP2 board via the instrument's rear panel. Switch 2017 off, remove the six panhead screws securing the board to the rear panel heat sink and pull out the board. Maintain the electrical connections and take care the board does not short circuit to the chassis. Switch on again and carry out the necessary adjustments.

(4) Check that the nominal +8.5 V supply is present, connecting the d.v.m. between the positive side of capacitor C2 (A0) and earth, see Fig. 6.

Master oscillator (AS1)

40. The master oscillator should whenever possible be serviced by the nearest Marconi Instruments service agent or Service Division, especially if an internal fault is suspected. However the following information is provided to assist in some of the rectification and re-alignment that may be attempted if it is not possible to return the instrument for repair. If attempting mechanical adjustments to the motor drive gear box assembly it should be noted that the socket head screws securing each of the two end stop cams are accessible to the user when the instrument has been tuned to the minimum and maximum frequencies on Range 8 (256 and 512 MHz) respectively. This convention should be maintained so that further re-adjustments at a later date may be made with ease.

41. Oscillator does not cover basic range (256-512 MHz, Range 8):- If this is the case carry out the following re-alignment procedure.

(1) Manually tune the oscillator to its lowest point i.e. when end stop restricts further movement. The frequency at this point should be approximately 248 MHz. If not, loosen the two motor gear box clamping screws to free the oscillator's fibre-glass plunger from the gear box assembly, these are shown in Chap. 7, Fig. 23, Item 23.

(2) Adjust the fibre-glass rod until a minimum frequency is noted, then further adjust the rod to note the maximum frequency it is possible to obtain. It should then be possible to fasten the rod plunger back to the gear box assembly so that when tuned to the minimum and maximum positions the frequency overlaps by equal increments of approximately 8 MHz above and below the required limits (256-512 MHz).

Note...

If the above re-alignment is carried out, end stop switches and the steering potentiometer RV1 will also need re-adjustment, this procedure is given in the paragraphs following.

42. End stop switch adjustment:- If the end stops operate at the incorrect frequency i.e. before the oscillator has reached either of its frequency limits 256 MHz or 512 MHz on Range 8, or if the fibre-glass connecting rod has been disconnected from the gear box for any reason it will be necessary to re-adjust the end stop switch operation.

(1) First tune the 2017 to a carrier frequency of ≈251 MHz on Range 8 manually then switch off the instrument and remove the Motor Drive Board AS7. Connect a multimeter set to the x1 ohms range to Board AS1B pins 1 and 3.

(2) Release the operating cam of micro-switch SBB from the end of the drive shaft taking care not to change the pre-selected frequency, rotate the end stop cam until the micro-switch SBB just operates and the multimeter reading changes from open circuit condition to approximately 100 Ω.

(3) Resecure the cam to the shaft and refit board AS7. Switch the 2017 supply ON and manually tune to a frequency of ≈516 MHz on Range 8. Then once more switch the 2017 supply OFF and again remove board AS7. Connect the multimeter to Board AS1B pins 1 and 2.

(4) Release the operating cam of micro-switch SBA and rotate the cam until SBA operates and the multimeter reading changes from open circuit condition to approximately 100 Ω. Resecure the cam to the shaft and once again refit board AS7.

43. Steering potentiometer RV1 adjustment:- If the VCOs, Range 9 do not change over at the correct frequency (approximately 710 MHz) or if the oscillator's fibre-glass connecting rod has been disturbed, RV1 will require adjustment. Proceed as follows:-

(1) Connect the multimeter positive terminal to the HORIZ OUT front panel socket and select a low d.c. volts range. Select a frequency of 256 MHz and check that a reading of 0.74 V is obtained on the multimeter. If this is not correct, locate the two part flexible coupling on the gear box assembly and the potentiometer RV1 wiper. The flexible coupling is shown in Chap. 7, Fig. 23, Item 8.

(2) Loosen the coupling at the gear box side and adjust the position of RV1 wiper to give the correct voltage, 0.74 V d.c. Re-secure the coupling and check that when the oscillator is driven up to the top of the range and returned to 256 MHz the HORIZ OUT output voltage again returns to 0.74 V d.c.

44. No oscillator output. A number of simple checks can be carried out to determine the serviceability of some of the oscillator components. These are as follows:-

(1) With a multimeter set to the ohms range connect the terminals to C17 and C22 filter output capacitors, these are situated on the top of the oscillator filter box and are connected to brown and yellow wire terminations.

(2) Disconnect SKBM from board AS5 and check that with the multimeter negative terminal connected to C17 and positive to C22 the varactor D1 is forward biased and reads approximately 1.2 kΩ and reversing the multimeter terminations gives open circuit. Connecting the multimeter between C17 and earth should read open circuit and similarly between C22

and earth. These checks confirm that C9, C10 and all the filter feed through capacitors are not short circuiting to earth.

(3) Transistor TR1 can be checked by removing SKDH on board AS1B and connecting the multimeter set to the ohms range, negative terminal to earth and positive terminal to pin 4 of AS1B. The meter should read approximately 1.5 kΩ. Transfer the positive terminal to pin 6 of AS1B, the multimeter should now read approximately 2.2 kΩ, and reversing the multimeter terminations ∝.

Divider chain (AA11)

45. Initially check that the input signal from the master oscillator is present at the input PLBX, level should be approximately 220 mV, frequencies 256 - 512 MHz. If this is satisfactory check the output at PLBZ for an approximate level of 400 mV on each of the seven relevant ranges listed in Table 6 below.

46. If there is no output on any range check the following:-

(1) Decoder output logic, this is negative true for the selected range, t.t.l. level converted to e.c.l.

(2) Check that the buffer amplifier TR1 to TR3 gives an output level of approximately 300 mV at D2/D3 junction and that this signal is present on the output bus transmission line.

(3) Check the 6 dB power splitter outputs are approximately 110 mV at PLBY if not, suspect TR4/5, and 400 mV at PLBZ, if not suspect TR6-8.

47. If the fault is peculiar to individual ranges or a succession of ranges check that the logic switching operates as shown in Table 6 below. Check using a spectrum analyser for successive frequency dividing and investigate any discrepancies. Also check that the gating diodes pass the signal to the output bus transmission line in a satisfactory manner.

TABLE 6 DIVIDER SWITCHING

Range	*Gating diodes*	*÷2 Dividers*	*Driver & gates*	*Frequency*
1 & 2	D2/D15/D14	IC3,7,9a,9b,12a,12b	IC4/6,8,10,11,13,14	4-8MHz
3	D2/D13/D12	IC3,7,9a,9b,12a	IC4/6,8,10,11,13	8-16MHz
4	D2/D11/D10	IC3,7,9a,9b	IC4/6,8,10,11	16-32MHz
5	D2/D9/D8	IC3,7,9a	IC4/6,8,10	32-64MHz
6	D2/D7/D6	IC3,7	IC4/6,8	64-128MHz
7	D2/D5	IC3	TR10/12	128-256MHz
8 & 9	D3	-	-	256-512MHz

Low-pass filters (AA31)

48. Confirm initially that the r.f. signal from Amplitude Modulator board AA21 is present at PLCJ, the input to AA31 board. Where an individual filter is suspected use a spectrum analyser to examine the second harmonic content using other serviceable filters for comparison. Ensure that the half-octave filter is selected via its associated 7.5 V Zener diode and that the filter is connected across the input and output bus via its two coupling diodes, for other symptoms see below:-

(1) Upper or lower half-octave fault. When the half-octave filters are inoperative on the upper filter bank only, check that the logic instruction for the upper half at PLCL pin 9 is 'low' and at IC1 pin 20, 'high'. Check that a 'low' output is present on one of IC1 pins 9 and 17. Similarly if the lower filter bank is faulty check that PLCL pin 9 is high and IC1 pin 20 'low', and that a 'low' output is present on one of IC1 pins 1 to 8. If not suspect IC1, TR1 or the VCO changeover line derived from AS1,R1. If the filters have been satisfactorily selected check that the output bus diode (D51 for upper bank or D52 for the lower bank) is serviceable.

(2) If the fault is common to all ranges and all the filters are being selected correctly check that the input stages TR4/TR5 and TR2/TR3 each give a gain of 5 dB and the output stage TR23-TR25 a gain of 10 dB.

Output amplifiers and ALC (AB2)

49. This board's pre-set components and output levels are set up in the initial manufacturing stage isolated from the instrument in a special jig. It is recommended therefore that if realignment is found to be necessary this is carried out by the nearest Marconi Instruments service agent, or the board be replaced by a serviceable item. However some fault finding assistance is given in the following section.

50. Faults most likely to occur are breakdown of chip components and transistors. Check along the signal path to ensure that the levels indicated in Chap. 7, Fig. 2 are correct, investigating any discrepancies. Replacement of faulty components will not necessitate realignment on the board but care should be taken to solder a replacement component into the same position as that vacated by the defective item.

51. The gain of the h.f. amplifier can be altered, should this be necessary via the series resistor R74 and parallel resistors R73 and R75. The board should give a total gain of 14 dB between PLCR and the output SKCY. Component values for R73-R75 enabling the gain to be varied are as follows:-

Stage gain	*R74 series resistor*	*R73/R75 parallel resistors*
3 dB	16 Ω	270 Ω
4 dB	22 Ω	220 Ω
5 dB	27 Ω	180 Ω
6 dB	39 Ω	150 Ω

52. The function and setting up procedure for pre-sets and SIC components are given briefly in Table 16, this information and the following tables of d.c. voltages 7 and 8 should enable the fault to be identified. Unless otherwise stated each measurement is taken with reference to chassis.

TABLE 7 AB2 DC VOLTAGES (ALC & HF AMP. SELECTED)

Measurement point	*Conditions/remarks*	*Voltage*
TR29e		24V ±0.5V
b		23.6V ±0.5V
c		23.3V ±0.5V
R122/R123		24V ±0.5V
TR31c		0V ±0.2V
TR32c		0V ±0.1V
TR33c		11.9V ±0.2V
TR26c	With R100 set to central pos'n.	20.7V ±0.5V
e		1.35V ±0.1V
b		2.25V ±0.25V
TR23c		9V ±0.5V
e		0.35V ±0.1V
b		1.25 V ±0.25V
TR22c	With R96 set to central pos'n.	8.5V ±0.5V
e		0.65V ±0.1V
b		1.4V ±0.2V
TR18c		7.8V ±0.5V
e		0.8V ±0.1V
b		1.5V ±0.2V
TR15c		6.6V ±0.5V
e		0.95V ±0.1V
b		1.7V ±0.2V
Junct. D27/D2	Carrier on	0.1V ±0.05V
Junct. D27/D2	Carrier off	11.7V ±0.5V
R11/R12		4V ±0.5V
Junct. R16/TR4e		9.5V ±1V
Junct. R17/TR5b		0.6V ±0.1V
"	hf $\overline{\text{FULL OUTPUT}}$ asserted	<0.1V
Junct. R17/R128		10.5V ±1V
"	hf $\overline{\text{FULL OUTPUT}}$ asserted	<0.2V
TP8		3.0V ±0.4V
TP10		11.9V ±0.2V
TP12	With Pulse mode or VOR/ILS selected	3.0V ±0.2V
TP14		23.2V ±0.5V
TP16		-11.9V ±0.2V
TP17		3.0V ±0.2V

TABLE 8 AB2 DC VOLTAGES (LF AMP. SELECTED)

Measurement point	*Conditions/remarks*	*Voltage*
C18		24V ±0.5V
TP1		11.8V ±1V
TP8		2.9V ±0.1V
TP17		3.65V ±0.3V
R22/R23		15.8V ±1V
Junct. TR9/R219		0.9V ±0.1V
across R30		0.9V ±0.1V
Junct. R122/R123		7.2V ±0.5V
TR31c		23.7V ±0.5V
TR32e		11.9V ±0.2V
TR33e		0V ±0.1V
between TP+ +ve and TP2 -ve	after a long settling time	between 40-350mV
IC2 pin 3		0.175V ±10mV
IC2 pin 2		0.175V ±10mV
Junct. R8/C5		between +0.1V and -3.5V

53. Possible ALC faults on this board can be identified better with the r.f. source removed. This can be conveniently disconnected by detaching PLBZ on board AA11. Tables 7 and 8 indicate voltages present when the r.f. is disconnected.

54. RF output incorrect at all levels.

(1) Check that the ALC instruction at TP15 varies between approximately +1 V and +2 V when the selected r.f. level is changed from +7.1 dBm to +13 dBm by the operation of the r.f. fine level control. If this is incorrect refer to the Fine Attenuator AS2/AS3 fault finding paragraph.

(2) Check that the linear control voltage is between 8.8 V and 9.5 V is present at D10 cathode, if not suspect IC4,IC5a.

(3) Check the h.f. channel amplifier circuit by selecting a carrier frequency greater than 4 MHz. Set the r.f. level within the range +7.1 dBm to +13 dBm and connect a d.v.m. to TP15. Adjust the r.f. level fine control to set an ALC instruction voltage of 2.0 V and maintain the setting for the following checks.

(4) Check that the voltage at TP21 is 0.685 V ±0.01 V and at TP13 it is 1.37 V ±0.2V.

(5) Increase the r.f. level coarse attenuator control by 6 dB and check that the d.v.m. reading at TP13 doubles.

(6) Reduce the r.f. level coarse attenuator to the minimum level being careful not to move the fine level control setting. Check that the voltage at TP13 is now 0.685 V ±0.01V and TP19 is 1.075 V ±0.003V. If any of the above voltages are incorrect suspect IC12 or IC8.

55. RF output incorrect at levels -125 dBm to +13 dBm (Full o/p).

(1) Check that the full output instruction is present at PLCW pin 3 and at TR49.

(2) After setting the ALC instruction voltage as described in the previous paragraph check that the voltage at TP21 is 0.685 V ±0.01 V and at TP13 is 1.37 V ±0.2 V. If either of these voltages are incorrect suspect TR49 or IC7b3.

56. RF output incorrect at levels +13 dBm to +19 dBm (Peak o/p).

(1) Set the ALC instruction voltage as described in para. 55 with the coarse and fine r.f. level controls, then increase the coarse r.f. level control a further 6 dB taking care not to move the fine control setting.

(2) Check that the peak output instruction is present at PLCW pin 4 and at TR50.

(3) Check that the voltage at TP21 is 1.37 ±0.2 V and at TP13 is 2.75 V ±0.2 V. If either voltages are incorrect suspect TR50 or IC7c3.

57. No r.f. output at frequencies 10 kHz - 4 MHz (Range 1).

(1) Check that the RANGE 1 $\overline{\text{ON}}$ instruction is present at TR30 emitter and that both TR30 and TR31 turn on to complete the +23 V line. Also check that TR29 and TR33 turn off to disable the h.f. amplifier.

(2) Set the r.f. coarse and fine level controls to give an ALC instruction voltage of 2.0 V at TP15. The voltage at IC2 pin 3 should then be 0.175 V ±0.1 V, similarly the voltage at IC2 pin 2 should be identical.

(3) Check that a voltage of between +0.1 V and -3 V is present on IC2 pin 6. If any voltages are incorrect suspect IC1, IC2 or TR1a2.

(4) Check that the r.f. 4 - 8 MHz signal is fed to AB1 via SKCP and that the frequency and r.f. levels through the stages of AB1 back to AB2, PLCX pin 7 are as indicated in Chap. 7, Fig. 2.

(5) Check the 10 kHz - 4 MHz signal through AB2 low noise amplifier TR2-TR4, check that TR6 gain increases by 6 dB when FULL OUTPUT is called for, and finally check the class A amplifier TR6 to TR12.

58. RF output incorrect on pulse modulation. In this mode of operation an ALC Store Update sequence operates for 30 ms when Pulse mode is initially selected. The sequence is also carried out whenever a significant shift in the generator operating frequency is made. IC3b2 switches from the closed to the open loop condition replacing the Error Drive voltage normally fed via IC6 by a stepped ramp voltage obtained instead from the ALC Store.

59. In the Pulse mode the r.f. level should be accurate to within ±3 dB, if this is not so the following checks will assist in the diagnosis of a fault. Each time a check is to be carried out on the ALC Store the 20 ms Update sequence must be operated, this can be achieved by changing the carrier frequency and observing the result on an oscilloscope. Alternatively it is possible to disconnect the ALC Update line by unsoldering one end of inductor L22 or L21 of

AB0 filter unit, this is adjacent to AB3 board. Apply +5 V to the free end connected to AB2 ALC Update line, this will give continuous operation of the ALC Store circuit and simplify fault location.

60. To confirm an ALC Store fault, initially connect a d.v.m. to TP8. The voltage here should be similar in both the Normal and Pulse mode operations, if not, use the oscilloscope to carry out the following checks:-

(1) Check that the 15 ms ALC UPDATE instruction is present on PLCW pin 1 when the 2017 carrier frequency is shifted by a significant amount. When this has been confirmed the +5 V supply can be connected to either L22 or L21.

(2) Check that a crude square wave, frequency approximately 60 kHz, is obtained at TP11. If not suspect TR41-TR48.

(3) Check that an upward ramp, amplitude 0 V to +8 V, pulse width between 1.8 and 3 ms is obtained at TP12. Expand the oscilloscope time base to observe the ramp steps. Check that each of the steps occur at similar intervals, if not suspect IC10.

61. After rectification remove the +5 V supply from the ALC Update line if this was connected and reconnect the inductor L22 or L21. Apply a d.c. voltage of +1.5 V to the 2017 PULSE MOD socket, set the r.f. level to 0 dBm and check that in the pulse modulation mode the level is within ±3 dB for carrier frequencies in the range 4 MHz to 1024 MHz.

Frequency (Unlock/Lock) domain faults

62. Faults in this area may be located by the use of one of the three following tables and the following procedure.

(1) External Counter mode only:- Check that the signal exists at SKAC on unit AL4.

(2) All other modes:- Check that the signal is present at r.f. output socket, if not refer to Tables 9, 10 and 11.

(3) Check that the INT/EXT 1 MHz STD switch is in the INT STD OUT position.

(4) Check all units and p.c.b's have the correct power supplies applied to them.

(5) Check that all relevant p.c.b's have the correct function control data applied (for AL4 and AL5 boards refer to Chap. 4-2, Tables 4 and 5).

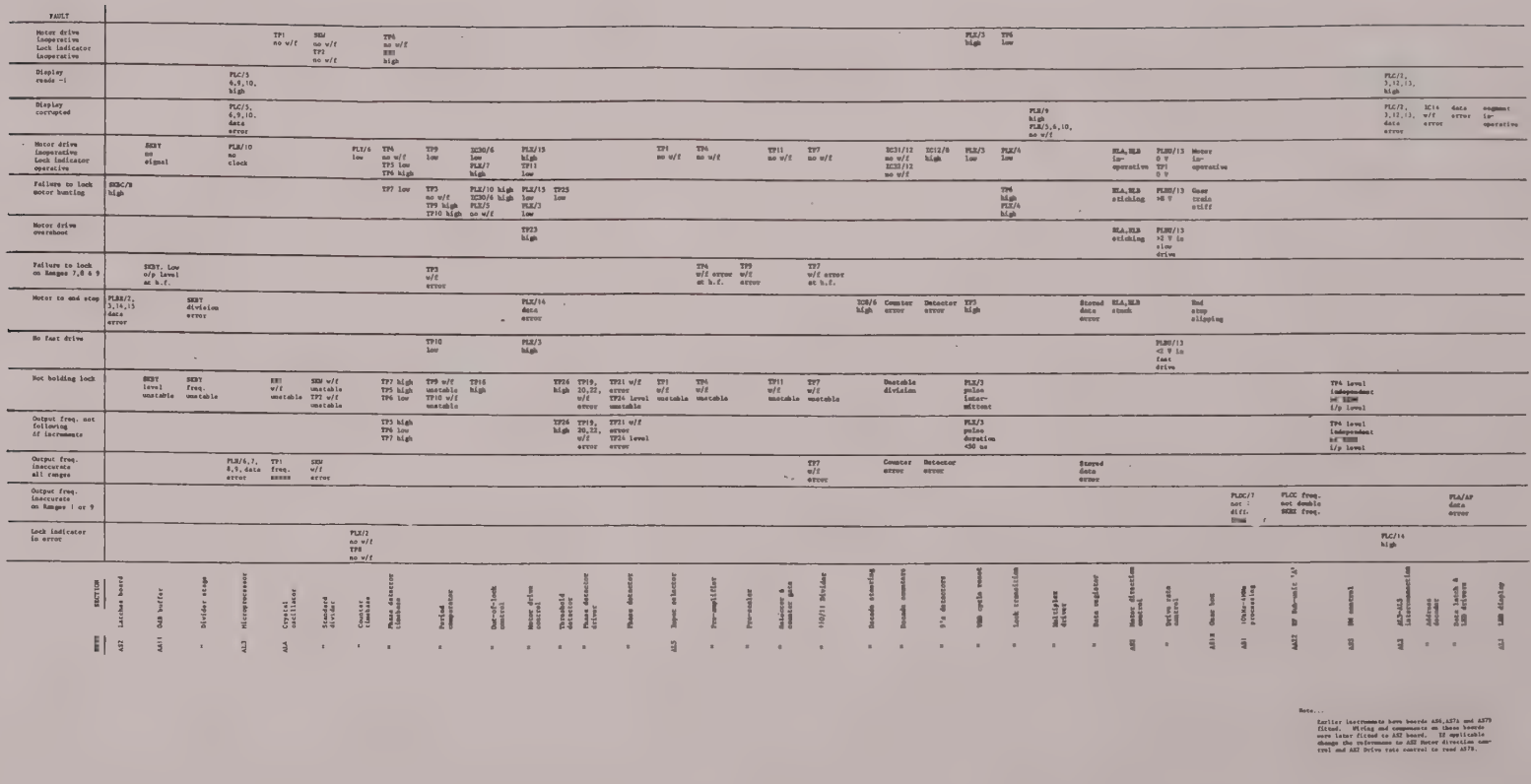
(6) Locate the fault condition by reference to the symptoms given in the left-hand column of each table. Check across the page from left to right with reference to the unit identification given at the foot of each table. At each relevant unit or section the level interconnection reference or test points are shown and with it the indicative fault condition.

(7) Faults in the SWEEP mode may normally be traced using the LOCK mode, Table 10. Sweep speed faults should be investigated on Motor Drive circuit.

TABLE 9 UNLOCK MODE FAULT ANALYSIS

FAULT	SECTION	UNIT	Dd8 buffer	Divider stage	Crystal oscillator	Standard divider	Counter timebase	Phase detector timebase	Out-of-lock control	Phase detector driver	Phase detector	Input selector	Pre-amplifier	Pre-scaler	Selector & counter gate	LSD decade counter	Decade steering	Decade counters	Range 1 subtractor	Multiplexer driver	Multiplexer	FM control	10kHz-4MHz processor	AL3-AL5 interconnection	Address decoder	Data latch & LED drivers	LED display	RF Sub-unit 'A'
			AA11	"	AL4	"	"	"	"	"	"	AL3	"	"	"	"	"	"	"	"	"	AE5	AE1	AL2	"	"	AL1	AA22
Freq. display seized					TP1 no w/f	SKW no w/f TP2 no w/f	FLY/8 no w/f FLY/10 no w/f												FLR/9 high FLR/5,6,10. no w/f					FLC/5,6 10, high FLC/11 high	IC14 o/p's all high			
Freq. display indicates -1																			TP15 high					FLC/2,3 12,13 high				
Freq. display indicates zero on all ranges	SKBY no signal						FLX/8 high FLY/16 low				TP1 no w/f	TP4 no w/f			TP13 no w/f	TP8 no w/f								FLC/2,3, 12,13 low				
Freq. display indicates zero on Ranges 1-6		SKBY frequency undivided					IC17/3 high								IC10/15 no w/f													
Freq. display indicates zero on Ranges 7-9							IC23/8 high TP8 high							TP9 no w/f														
Freq. display erroneous on all ranges		SKBY level <50mV	TP1 freq. error	TP2 w/f error SKW w/f error	w/f error						TP1 w/f error	TP4 w/f error			TP13 w/f error	IC14 outputs w/f error	IC8/3 w/f error	Decade outputs w/f error	IC24/8 IC26/13 w/f error	FLR/5, 6,9,10. w/f error	FLJ/6,7, 9,10. data error			FLC/2,3 12,13 data error	IC14 w/f error	Data error	Segment in-operative	
Freq. display erroneous on Range 1 only					IC17/3 w/f error													IC24/8 IC26/13 w/f error				FLDC/7 is not 4MHz different from FLDF					
Freq. display erroneous on Ranges 1-6					IC17/3 w/f error																							
Freq. display erroneous on Ranges 7-9					IC23 w/f error								TP4 w/f error at h.f.	TP9 w/f error														
Freq. display erroneous on Range 9 only					IC38 low																							PLCC freq. not double SKBZ freq.
Excessive FM distortion								TP5 no w/f TP6 no w/f	TP19, 20,22, w/f error	TP21 w/f error TP24 level not 10.0V											TP4 level not 24.0V							
Random freq. display								TP4 no w/f	FLX/7 low																			

TABLE 10 LOCK MODE FAULT ANALYSIS



Note...
Earlier instruments have boards A56,A57A and A579 fitted. Wiring and components on these boards were later fitted to A57 board. If applicable change the references to A56 Motor direction control and A57 Drive rate control to read A579.

TABLE 11 EXTERNAL COUNTER MODE FAULT ANALYSIS

FAULT	Crystal oscillator AL4	Standard divider "	Counter timebase "	Input selector AL5	Pre-amplifier "	Schmitt-trigger "	Pre-scaler "	Selector & counter gate "	LSD decade counter "	Decade steering "	Decade counters "	Range 1 subtractor "	Multiplexer driver "	Multiplexer "	AL3-AL5 interconnection AL2	Address decoder "	Data latch & LED drivers "	LED display AL1
Freq. display seized up	TP1 no w/f	SKW no w/f TP2 no w/f	PLY/8,10 no w/f										PLH/9 high PLH/5,6,10 no w/f		PLC/5,6,10 high PLC/11 high	IC14 o/p's all high		
Freq. display indicates -1			PLY/6 high								TP15 high				PLC/2,3,12, 13, high			
Freq. display indicates zero on all ranges			PLX/8 high PLY/6 low					TP13 no w/f	TP8 no w/f						PLC/2,3, 12,13 low			
Display indicates zero 10Hz-10MHz range only						TP10 no w/f												
Display indicates zero 1-100MHz range only								IC10/15 no w/f										
Display indicates zero 10-500MHz range only			IC23/8 high				TP9 no w/f											
Display indicates zero 10Hz-10MHz & 1-100MHz ranges			IC17/3 high															
Display indicates zero 1-100MHz & 10-500MHz ranges				TP1 no w/f	TP4 no w/f													
Display erroneous on all ranges	TP1 freq. error	SKW w/f error TP2 w/f error	w/f error					TP13 w/f error	IC14 outputs w/f error	IC8/3 w/f error	Decade outputs w/f error	IC24/8, IC26/13 w/f error	PLH/5,6 9,10, w/f error	PLJ/6,7, 9,10, data error	PLC/2,3, 12,13, data error	IC14 w/f error	data error	segment inoperative
Display erroneous on 10Hz-10MHz range only	IC12/6 not 100Hz					TP10 w/f error												
Display erroneous on 1-100MHz range only								IC10/15 w/f error										
Display erroneous on 10-500MHz range only			IC23/8 w/f error				TP9 w/f error											
Display erroneous on 10Hz-10MHz & 1-100MHz ranges			IC17/3 w/f error															
Display erroneous on 1-100MHz & 10-500MHz ranges				TP1 w/f error	TP4 w/f error													

TABLE 12 AL4 TEST POINTS

Test point ref.	*Function*	*Circuit description*	*Remarks*
TP1	10 MHz	Standard divider	Crystal oscillator output
TP2	1 kHz	Standard divider	Repetitive clock to counter timebase
TP3	Comparator clock	Period comparator	Repetitive clock, range and state dependent period
TP4	Datum pulse	Phase detector timebase	Repetitive clock (100 Hz)
TP5	Bias pulse	Phase detector timebase	Repetitive clock (100 Hz)
TP6	Ramp pulse	Phase detector timebase	Repetitive clock (100 Hz)
TP7	Threshold pulse	Phase detector timebase	Repetitive clock (100 Hz)
TP8	6.25 Hz	Lock indicator control	Intermittent clock, state dependent
TP9	+ 0.05% / - 0.10% Threshold	Period comparator	Clock, variable pulse-width and period
TP10	±1% threshold	Period comparator	Clock, variable pulse-width and period
TP11	Out of lock	Out-of-lock control	State dependent logic
TP12	Delayed out-of-lock	Out-of-lock control	State dependent logic
TP13	Gate reset $\overline{\text{enable}}$	Counter timebase	Repetitive clock, range dependent period
TP14	Set pulse, Mode transition	Out-of-lock control	Single shot pulse
TP15	Set pulse, Lock transition	Out-of-lock control	Single shot pulse
TP16	$\overline{\text{In lock}}$	Out-of-lock control	State dependent logic
TP17	-	-	-
TP18	In lock	Out-of-lock control	State dependent logic
TP19	Ramp sample pulse	Sample and hold driver	Repetitive clock, state dependent period
TP20	Delay pulse	Sample and hold driver	Repetitive clock, state dependent period
TP21	Ramp waveform	Sample and hold circuit	Fixed period, variable waveform
TP22	Transfer pulse	Sample and hold driver	Repetitive clock, state dependent period
TP23	Drive $\overline{\text{inhibit}}$	Motor drive control	Single shot pulse
TP24	Fine freq.control	Sample and hold circuit	DC level state dependent
TP25 / TP26	Out-of-threshold	Threshold detector	State dependent logic
TP27	$\overline{\text{CW}}$ drive	Threshold detector	State dependent logic

TABLE 13 AL5 TEST POINTS

Test point ref.	*Logic level*	*Function*	*Circuit description*	*Remarks*
TP1	-	Input selector output	Input selector	RF signal, f int. or f ext.
TP2	-	Pre-amplifier input	Pre-amplifier	RF signal, f int. or f ext.
TP3	TTL	Data strobe	÷10/11 Programmer	Clock, variable pulse width and period
TP4	ECL	Pre-amplifier output	Pre-amplifier	Repetitive clock at f int. or f ext.
TP5	ECL	Pre-scaler input	Pre-scaler	Repetitive clock at f int. or f ext.
TP6	TTL	Trigger	Lock transition circuit	Single shot pulse
TP7	TTL	÷10/11 output	÷10/11 Programmer	Repetitive clock, signal dependent pulse width and period
TP8	TTL	First decade output	Counter first decade	Repetitive clock, signal dependent period
TP9	ECL	Pre-scaler output	Pre-scaler	Repetitive clock at f int./4 or f ext./4
TP10	ECL	Schmitt trigger output	Schmitt trigger	Repetitive clock at f ext. ≤10 MHz
TP11	ECL	Selector output	Selector	Repetitive clock, signal dependent period
TP12	ECL	VRD input	÷10/11 Programmer	Repetitive clock, signal dependent period
TP13	ECL	Counter gate output	Counter gate	Clock, signal and state dependent period
TP14	ECL	Counter input	Counter first decade	Clock, signal and state dependent period
TP15	TTL	MUX strobe	Range 1 subtractor	State dependent logic
TP16	ECL	Pre-amplifier output	Pre-amplifier	Repetitive clock at f int. or f ext.
TP17	ECL	Selector input	Selector	Repetitive clock at f int. or f ext.

Note...

Board AL5 has both ECL and TTL logic levels, board AL4 has exclusively TTL. Typical values for both are as follows:-

	TTL	*ECL*
V high	3.4 V	-0.4 V
V low	0.35 V	-2.1 V

Coarse attenuator (AT0)

63. If a coarse attenuator fault is suspected, first check that the attenuator pads operate in the correct sequence, for details see Coarse attenuator functional check.

(1) If none of the relays are operating check that the +8.5 V unregulated supply is present.

(2) If relays are operating check that the pads are in or out of circuit according to the table given on the circuit diagram in Chap. 7. (Pads not in circuit are switched out by completing an earth return via board AS4 energizing the relay.)

(3) If the incorrect pads are in circuit for any given coarse attenuator setting, check that the logic on board AS4 at the junction of PLBD and R9, R13, R15, R17 is according to that given in Chap. 4-2, Table 1. If the instructions are incorrect suspect a fault on board AS4, or the logic applied to it.

Note...

The v.s.w.r. of the attenuator is optimized using adjustable flags in the attenuator. If an attenuator microswitch or resistor is to be replaced this may affect the flags and so the setting up of the attenuator requires the use of accurate v.s.w.r. and attenuator measuring equipment. In case of difficulty further assistance may be obtained from Marconi Instruments' agents or Service Division.

Fine attenuator (AS2/AS3)

64. If the fine attenuator operation is suspect proceed as follows:-

(1) Check the operation of both the manual front panel 6 dB fine control and the keyboard selection. If the fault is common to both modes of operation check the +24 V, +12 V, +5 V and -12 V d.c. supplies to the A-D and D-A converters on board AS3. The board can be placed in a more accessible position by means of an extender lead Code no. 43129-618W and a 14-way extender cable Code no. 43129-591M, part of the Optional accessories maintenance kit.

(2) Check that the correct logic instructions are present on AS3, PLBB pins J to M and 8 to 11, if this is not correct suspect a fault associated with the Microprocessor board AL3 interconnections.

(3) If the instructions from AL3 are correct check that the ALC instruction voltage is present at board AB2, PLCW pin 16 and is between +1 V and +2 V. If this is incorrect, check the function of the D-A converter IC9 and IC10.

(4) If only the manual front panel FINE LEVEL control is suspect check that the A-D reset ramp is present on pin H, and also the function of the A-D converter TR2-TR4 and IC8. Select via the front panel keyboard control a level of 100 µV e.m.f. then select ROTARY and check that the FINE LEVEL potentiometer gives a range of between 56 - 144 µV e.m.f. If necessary adjust R1 and R2 on AS3 to achieve this, these controls are interactive.

ALC limits

65. Two l.e.d. displays are situated on board AS4. These indicate when lit that the ALC voltage limits have been exceeded. The ALC voltage for range 1 frequencies is derived on board AB1 and for ranges 2 - 9 on board AB2. The upper limits l.e.d. D2 will light if the voltage is in excess of 6.2 V (when the r.f. output is low) and D1 will light if the voltage falls below 0.6 V (r.f. output is too high). Further assistance on possible ALC faults can be found in the output amplifiers and ALC (AB2) section.

Microprocessor control circuits (AL3/AS2)

66. The Microprocessor board AL3 is extremely reliable and the possibility of faults developing on the board itself are remote. The most likely cause of breakdowns are open circuit or intermittent connections between the Latches board AS2 and associated filter units. In searching for possible faults a logic probe should be used, set to accept TTL logic levels, 0 V and +2.4 V d.c. to obtain the necessary logic state information. If front panel functions are impaired

(1) Check each of the keyboards AK1, AK2 and AK3 for the correct operation and relevant interconnections.

(2) Check the interconnecting plugs and sockets on Latches board AS2 for indications of rapid logic activity, investigate the cause of any shown to be inactive.

(3) Check address and data lines for open or short circuits.

(4) Check clock out frequency is 3.072 MHz at AL3 PLH pin 10.

Note...

If plug in type IC's or PROM's are for any reason removed from the board ensure that extreme care is taken to avoid bending the spring tensioned sockets when the replacement of these is attempted.

Keyboard and display failures

67. Initially establish whether the fault is caused by the microprocessor system, display or keyboard. If a single key or a row or column of keys are inactive it is likely that it is a keyboard fault or a failure on the horizontal or vertical function data lines. If the display does not assume the initial status mode i.e. carrier frequency 400 MHz, no a.m. or f.m. and minimum r.f. level then a microprocessor fault may be suspected. In this event, read the paragraphs on microprocessor control circuits AL3/AS2. If a single seven-segment display has failed or a l.e.d. is not lit, a Display Driver AL2 or Display Unit AL1 fault is likely. Proceed as follows:-

68. Keyboard failure AK1/AK2:- Determine the number of inactive keys and check the following:-

(1) A 'low' instruction is arriving at both the vertical and horizontal function data lines on AK1, PLAY when a key is pressed. If not suspect open circuit diodes or +5 V supply.

(2) If l.e.d's are not lit check the function data to AK2, PLBK and that the 4-10 line decoder is being forced 'low' on each range selection and that the load resistor and l.e.d. is serviceable.

(3) If vertical and horizontal function data is present on each row and column of AK1, PLAY when the keys are pressed, check the interconnections through to AS2 Latches board, PLAY and check IC1 and IC2 latch outputs on this board.

(4) Finally check that the function data is in turn fed via AS2, PLT to the Microprocessor AL3 through AL0 filter unit X2.

69. Display failure AL1/AL2:- Initially substitute a known serviceable item for any individual seven-segment l.e.d. not functioning. If this has not failed the problem is likely to be caused by missing address/data logic from board AL2. If no l.e.d's are functioning, check that the unregulated +8.5 V supply to AL1, SKA, pin A is present, if not check connections to AL2 and AL3.

70. If the fault is restricted to either modulation or r.f. level functions or part of either function check the b.c.d. address to AL2, 1 of 10 decoder IC52, inverters IC37a3, IC51 and the relevant quad latches. Also check that the data from the Microprocessor AL3 is being fed to the addressed quad latch via PLE and to the Display unit AL1 via the decoder/driver, load resistor and PLB.

71. If the fault is restricted to the frequency display or part of it, check the b.c.d. address to AL2, 1 of 10 decoder IC14, inverters IC9, IC20 and the relevant quad latches. Check that the LATCH GATE $\overline{\text{OPEN}}$ instruction is present to IC9/IC20 via PLC pin 11. If not suspect board AL4/AL5 and turn to the paragraphs on Frequency (Unlock/Lock) domain faults. Check that the data from the Microprocessor AL3 is also being fed to the addressed quad latch via PLC and the quad latches. Finally check the decoder/driver, load resistor and the interconnection PLA.

72. Supplementary front panel l.e.d. faults:- Check that the l.e.d. and its supply are correct then check that the serial in data and the clock pulses on pin 1 and pin 8 of each parallel-out-serial-in registers are present. Check that each of these registers are being pulsed in turn by the Microprocessor AL3 (for further details see Chap. 4-2, para. 220) and that the relevant inverters give an output to the l.e.d. via either PLA or PLB.

AM faults

73. Assuming that the output frequency is correct and r.f. level accuracy and harmonic distortion is within specification the following checks will assist in diagnosing the fault.

74. Modulation oscillator (AK4):- Check that the internal modulation oscillator operates at all frequencies and at the correct level i.e. approx. 5.5 V p-p from the front panel MOD FREQ OUT (600 Ω) socket. Check that the signal is also fed via SAY, SAX, FM INT/EXT, AM INT/EXT switches, through AS2, PLDR pin 2, SKBD pin M to AS4, PLBD pin M.

75. If the oscillator fails to function on any range, check the signal is present at AK4, IC3, pin 2. If not suspect the oscillator IC3 or the buffer IC2. If the output is present but of the incorrect level, suspect photo coupler X1b2, diodes D1-D5 or output amplifier IC4. If only one of the frequency selections is at fault suspect range switch SA or the FREQ CONTROL potentiometer R3. If the remote selection is at fault, suspect IC1, TR1 or TR2.

76. AM control circuit (AS4):- Select AM INT, 99% AM DEPTH, MODULATION OSCILLATOR 1 kHz, AM ON, and check that a 1.5 V p-p 1 kHz sine wave exists at AS4, SKDT. Re-select different values of AM DEPTH, checking that the voltage level is reduced accordingly. If not suspect data from AS2, AL3, at PLBD pins 5-8, F-K, or alternatively the D-A converter IC1, IC2 and output amplifier IC3. Also check that (AM ON) relay RLA functions.

77. Amplitude modulator (AA21):- Check that with AM ON the controlled mod. signal is present at TP7, if not suspect AA22, 500 kHz filter.

Pulse modulation faults

78. If it is not possible to obtain pulse modulation at all, the fault is likely to lie within amplifiers AA24 and AA23. Connect an external 1 kHz signal to the PULSE MOD 50 Ω IN socket with an amplitude greater than 1 V p-p and select PULSE MOD ON. Check with an oscilloscope that these d.c. amplifiers operate by following the signal path through from AA24 tag 2, IC1a3 and tag 6 to AA23 tag 2, TR2, TR3 and tag 3.

79. If the carrier suppression ratio is suspect carry out the following checks:-

(1) Remove box AB0 and the external signal previously connected to the PULSE MOD 50 Ω IN socket, re-attach AB0 by means of extension leads and select CARRIER FREQ 80 MHz, RF OUTPUT 19 dBm, PULSE MOD OFF.

(2) Connect a spectrum analyser (20 kHz span) to PLCK output socket of AA31 board.

(3) Note the level, then select PULSE MOD ON and check that the residual signal is now at least 70 dB down on the original level. Repeat this check at a carrier frequency of 512 MHz, here the residual signal should be at least 54 dB down.

(4) Adjustment of the carrier suppression can be carried out by rotating AA21, R121 fully clockwise then with PULSE MOD ON turn R121 counter-clockwise until maximum suppression is obtained for both carrier frequencies. Possible causes of insufficient suppression are (i) connector AA2, PLCB to AA21 SKCB outer braiding broken away (ii) spring loaded clips on AA31 board coupling AA22 board loose, or incorrectly positioned (iii) spring retaining clips on AA21 mixers X1 and X2 not making a good contact.

(5) Pulse modulation off state can also be adjusted by the following method if required:-

Disconnect AA23 tag 3 connection from SKCD and connect instead an ammeter between tag 3 and earth (positive lead to tag 3). Adjust AA23, R3 for a current of 1 μA then re-connect tag 3 to SKCD, use low resistance leads to the ammeter.

RF amplifier level control (AA21)

80. It is possible that the r.f. level output from this board could be in error. If this is suspect, remove AB0 box and re-attach it to the instrument externally by means of extension leads. Unfasten AA31 board, removing the six panhead screws and five spring contacts (care must be taken to reposition these correctly on re-fitting, for details see RF Section (AA0) access). Leave AA31 board connectors attached so that the board may be lifted when access to AA21 is required. Alternatively remove AA31 and reconnect externally by means of extension leads in the same way as AB0 box, then carry out the following checks:-

(1) Connect an r.f. voltmeter to AA31 output SKCK, select 2017 CARRIER FREQ 50 MHz, RF LEVEL -127 dBm, and check that the level at SKCK is -7 dBm ±3 dB.

(2) Reselect RF LEVEL to -120 dBm to exert the h.f. $\overline{\text{FULL OUTPUT}}$ instruction which in turn causes RLB to energize and the level at AA31, SKCK to increase by 6 dB ±0.3 dB. If not suspect the h.f. $\overline{\text{FULL OUTPUT}}$ instruction line to AL3, relay RLB, or attenuator R105 - R107. Also check that the d.c. voltage at TP16 is +4.6 V ±0.05 V (set by R62) and that the error drive voltage and current settings at TP21, TP18 and TP19 are correct. Details of these are given in the auto levelling circuit, realignment section.

(3) Re-select RF LEVEL to +19 dBm and check that the level at AA31, SKCK is increased by a further 6 dB from that noted in step (2). If not suspect IC2, TR23 or D8. Also check that the d.c. voltage at TP16 is double that measured in step (2), if not suspect PEAK OUTPUT instruction line from AL3.

TABLE 14 AA21 TEST POINTS

Test point ref.	*Description/function*	*DC voltage w.r.t. chassis*
TP1	Range 9 on/off & VCO selector	
TP2	Freq. ranges 1-8	-10V ±1V
	Freq. range 9	+11V ±0.4V
TP3	Ranges 1-8	From +4.5V l.f. to +14.8V h.f.end
	Range 9	From +2.6V l.f. to +12.8V h.f.end
TP4		+11V ±0.05V
TP5		+10.5V ±0.05V
TP6	Set Mod. bias current	+4.6V ±0.2V
TP7	Controlled mod. signal	0V
TP8		+10.4V ±0.05V
TP9		+9V ±0.1V
TP10	Error drive voltage (typically +3V)	+1V to +6V
TP11		+9.3V ±0.1V
TP12		+9.3V ±0.1V
TP13/14	Used in initial manufacturing stage only	
TP15		+24V ±1V
TP16	AM (normal output) selected	+4.6V ±0.05V
	Pulse mod.	approx. 2mV
TP18	Auto levelling circuit	+12V ±0.5V
TP19	Auto levelling circuit	+10.6V ±0.3V
TP20		0V to +4V
TP21	For detaile see Error Drive Settings Table 15	
TP22		+24V ±1V

FM control faults (AS5)

81. The f.m. drive system is complicated by control systems for achieving wide and narrow deviation with both coarse and fine adjustments. It is important therefore to establish which part of the f.m. control system is not functioning. The checks given below are therefore devoted to identifying which area is at fault. If it is necessary to carry out re-alignment of this board after repair, turn to the paragraphs relating to FM Pre-distortion alignment (AS5).

(1) Check the -12 V, +12 V, +24 V and +70 V d.c. supplies.

(2) Check that each of the f.m. coarse and fine 11-bit binary instructions are present at PLBC when selected on the front panel FM DEVIATION controls. The maximum deviation being dependent on the r.f. range in use (for details see Performance data).

(3) Check that the fine frequency control voltage (between 0 V and +20 V) is present at SKBN and is summed with the fine tune control voltage at IC8 pin 6.

(4) Check that the FM ON instruction at PLBC pin B has energized RLA via TR11. If any of the instructions above are absent suspect AS2 or AL3.

82. Wide deviation.

(1) Check that RLE is de-energized and continuity exists through its contacts.

(2) Check that RLF is de-energized and the linear network TR23-TR34 is connected via RLFa2 and that 0 V is applied to PLBM pin 7 via RLFb2.

83. Narrow deviation.

(1) Check that RLE energizes and that the 30 dB attenuator R100-R102 is serviceable when switched in.

(2) Check that RLF energizes removing the linear network TR23-TR34 via RLFa2, and that RLFb2 operates changing the voltage at PLBM pin 7 from 0 V to a proportion of IC8 pin 6 output.

(3) Check the fine control D-A converters TR1-TR9, m.s.b's, and IC4-IC6, 8 l.s.b's. The output at IC1 pin 6 should reflect a voltage proportional to the current of the summing bus.

84. Coarse control

(1) Set the front panel FM DEVIATION controls to give a level '1' instruction to PLBC pin 8, this should cause RLB to energize via TR12 to give 10 dB attenuation at IC7 pin 2. Further check that a level '1' instruction to PLBC pin K gives a further 10 dB attenuation via RLC and finally that a level '1' instruction to PLBC pin 9 gives another 10 dB attenuation via RLD. If not suspect TR12-TR14, relays RLB, RLC or RLD or resistor loads R68, R69, R70.

(2) Check that IC9 summing amplifier pin 3 has a fixed +6.15 V d.c. applied and pin 2 has a similar voltage.

(3) Check that a gain of approximately 2.4 is obtained through the class B amplifier TR16 - TR22.

85. Excessive residual f.m. Residual f.m. is usually to be found in one of three areas described as follows:-

(1) Although the Master oscillator AS1 is a low noise type and spurious f.m. components are normally of a very low order it is possible that the mechanical fit of oscillator components could be such as to cause vibration to set up on the oscillator due to the action of the cooling fan.

(2) Varactor diode D1 whose sensitivity can be up to 10 MHz/V and the +70 V d.c. supply may also be a cause of trouble. Wherever possible a fault in the master oscillator unit should be rectified by the nearest Marconi Instruments service agent or Service Division.

(3) There should be few significant mains related spurious signals from AP2. The +70 V supply voltage should be within ±0.5 V and all other d.c. supply regulators, within 10% of their nominal value. The level of ripple for all these supplies should be typically 1 - 2 mV. In these areas a fault is most likely to be caused by the breakdown of an isolated component. Each external load can be disconnected if necessary from the regulators via PLAM, PLBJ, PLAH or PLAN as required to eliminate the possibility of a breakdown on the output side.

RF signal leakage

86. If the radiated r.f. signal is out of specification identify the general location of source and try to identify, if possible, the unit. Problems can be caused by damaged gaskets, distorted lids, insulated screws, damaged r.f. connectors and damaged coaxial cables.

GPIB faults

Test equipment : items x, Bus fault analyser
y, GPIB lead assy.

87. With 2017 power OFF set all five address switches and the TON switch to '1'. Switch 2017 power ON and check that 1__11111 is displayed in the CARRIER FREQ window. The display will be replaced after several seconds by the local operating mode condition, also check that the front panel ADDRESSED l.e.d. is lit.

88. Switch the power OFF again and set the TON and address switches to '0'. Switch power ON and check that the CARRIER FREQ display now shows 00000 and the ADDRESSED l.e.d. is not on, again this will be replaced after several seconds by the local operating mode condition.

89. The following procedure will assist in diagnosing a fault within the 2017. Disconnect any equipment from the rear panel GPIB socket and connect instead the bus fault analyser by means of a GPIB lead (this can be supplied as an optional accessory Code No. 43129-189U if required). Use of the

analyser is especially helpful in the diagnosis of GPIB faults in that bus commands can be sent to assert IFC, REN, ATN, EOI and SRQ. The talker/listener NRFD, DAV and NDAC handshake procedure can also be satisfactorily checked.

90. To check NRFD and NDAC lines select the 2017 address and TON switches to '0' and set the ICS analyser controls to the following:-

(1) MEM OFF; LOOP MODE OFF; COMP MODE OFF.

(2) TALK/LIST/MEM PROG to TALK.

(3) SINGLE STEP/SLOW/FAST to SINGLE STEP
REN to '1'
SRQ to '0'
EOI to '0'
ATN to '0'
DIO to 0010, 0000

(4) Press and release the IFC control.

Note...

Analyser NRFD and NDAC l.e.d's are off, if not trace the above lines from the GPIB rear panel socket on board AG1, SKR pins 7 & 8, IC6a, IC7a, PLDV pins 11 & 12 through AL0 high speed filters C1, C7L1/C2, C8,L2 to AL3, PLN pins 7 & 6, IC1 and IC6 talker/listener pins 37 & 38.

91. To check the REN line maintain the 2017 address and TON switch selections and set the ICS analyser controls as follows:-

(1) ATN to '1'.

Note...

NDAC l.e.d. should be on, NRFD l.e.d. off.

(2) Press and hold 'STEP' button.

Note...

NRFD and DAV l.e.d's are on, NDAC l.e.d. off.

(3) Release 'STEP' button.

Note...

NDAC l.e.d. is on, NRFD and DAV l.e.d's off, 2017 ADDR & REM l.e.d's both on. If only REM l.e.d. is on suspect the ADDR l.e.d. or +5 V supply voltage to it. If both REM and ADDR l.e.d's are off this indicates an incorrect DIO pattern. In this event reselect each of the ICS analyser DIO lines to '1' individually and trace from AG1, SKR, IC3, IC4, IC5, PLDV and PLS to AL0 filter unit X4 then AL3, PLP, IC5 and IC6 pins 28 to 35. If only ADDR l.e.d. is on then suspect a REN line fault, check from AG1, SKR pin 17, IC2, PLS pin 13 to AL0 filter unit X4, C2 then AL3, PLP pin 7, IC4 and IC6 pin 25.

(4) If step (3) was satisfactory set REN to off and check that the 2017 REM 1.e.d. is off and ADDR 1.e.d. remains on.

92. To check IFC line, maintain the previous 2017 settings.

(1) Press and release the ICS analyser IFC button.

Note...

The 2017 ADDR 1.e.d. should then be extinguished. If not suspect the IFC line and check from AG1, SKR, pin 9, IC2, PLS pin 13, to AL0 filter unit X4,C3 than AL3, PLP pin 9, IC4 and IC6 pin 24.

93. To check the SRQ line maintain the previous 2017 settings and apply a 5 V d.c. to the RF OUTPUT socket causing the RPP circuit to trip. This action will in turn cause the ICS analyser SRQ 1.e.d. to light. If not check the SRQ line from AG1, SKR pin 10, TR3, PLS pin 14, to AL0 filter unit X4,C4 then AL3, PLP pin 6, IC4 and IC6 pin 27.

94. If the above tests are carried out and no fault condition is apparent check the T/$\overline{R}$1 and T/$\overline{R}$2 lines from AL3, IC6 pins 1 and 2, IC2, IC3, PLN pins 5 and 2 to AL0 high speed filters C3, L3, C9/C6, L6, C12 then AG1, PLDV pins 13 and 16. Each instruction should then be checked to the drivers and transceivers on board AG1.

REALIGNMENT

95. This section contains information for the overall realignment of the instrument. Preset components and bay numbers are indicated in Chap. 7 Servicing diagrams.

Note...

Before any adjustments are made all screening covers should, where possible, be firmly fitted.

96. After completing repairs it may be necessary to realign affected circuits. Any adjustments additional to those detailed in this section should be carried out only after consulting Chap. 4-2 and the circuit diagrams in Chap. 7. If the full overall realignment procedure is not required, individual steps may be performed providing they do not interact with other adjustments. It is recommended that the effects of any readjustment are always considered with reference to the circuit diagrams.

97. Test equipment required. Refer to Table 1 for the list of test equipment required.

Input offset null adjustments (AB2)

98. Should IC8, IC9 or IC12 integrated circuits require replacement it will be necessary to adjust these when fitted to obtain the lowest possible value of input offset voltage. This can be achieved by the following procedure:-

(1) Disconnect the r.f. source from AA11 board PLBZ, and in each case connect a d.v.m. set to the 2 V d.c. range to the test points indicated below.

(2) IC8: Connect the d.v.m. positive lead to TP18 and the negative to TP17, adjust R151 for a d.v.m. reading of less than 1 mV. Set the ALC instruction voltage at TP15 to 2.0 V by means of the r.f. level coarse and fine controls then check the voltage at IC8 pin 6, note the reading (a). Now check and note the voltage at TP13(b), this should be 0.685 V ±0.01 V. Subtracting (a) from (b) should give a value of 3 V ±0.3 V. This voltage should also be present on TP7 and TP8.

(3) Connect the d.v.m. positive lead to TP3 and the negative to TP19. Adjust R153 for a reading of less than 3 mV.

(4) IC9: Connect the d.v.m. positive terminal to D15 cathode and the negative to TP16, adjust R159 for a d.v.m. reading of less than 1 mV.

(5) IC12: Connect the d.v.m. positive terminal to TP21 and the negative to TP20. Adjust R213 for a reading of 1 mV.

FM pre-distortion alignment (AS5)

Test equipment : items g, Distortion factor meter
h, AM/FM modulation meter
i, AF oscillator
p, 100 MHz oscilloscope with plug-in capability
r, Differential amplifier

99. Connect board AS5 to the extender lead Code no. 43129-620S, part of the optional accessories maintenance kit. Set the 2017 CARRIER FREQ to 19 MHz (unlocked), FM DEVIATION of 160 kHz, EXT FM UNLEVELLED, MODULATION OSCILLATOR OFF, FM ON.

100. (1) Disconnect the fine freq sync drive from SKBN and connect a variable d.c. external power supply to SKBN and set this to give +10 V d.c. sync drive.

(2) Connect a low distortion a.f. oscillator to the 2017 600 Ω IN socket, select a modulation frequency of 70 Hz and an approximate level of 750 mV. Set 2017 FINE TUNE potentiometer to mid-travel.

(3) Insert a differential amplifier into the oscilloscope main frame and connect the remaining test equipment as shown in Fig. 14 below.

(4) Initially switch off the external a.f. source and connect a multimeter selected to a suitable d.c. volts range across TP2 and TP3. Check that this reads 0.17 V ±0.02 V, if not adjust R1 for this figure.

(5) Connect the multimeter between TP6 and earth and adjust the variable d.c. source to give 0 V.

(6) Connect the multimeter between TP4 and earth, adjust R2 for +24 V ±0.2 V, switch external modulation source on and set to a suitable level. Tune the TF 2300B to the carrier frequency and select f.m. deviation. Adjust the oscilloscope controls to observe the diagonal trace this could have a hockey stick effect if alignment is required. Adjust R7 to R11 in ascending order for the best straight line. If necessary increase the a.f. source level to enable more effective adjustment of R10, R11. Next adjust R6 to R2 in descending order for the best straight line presentation.

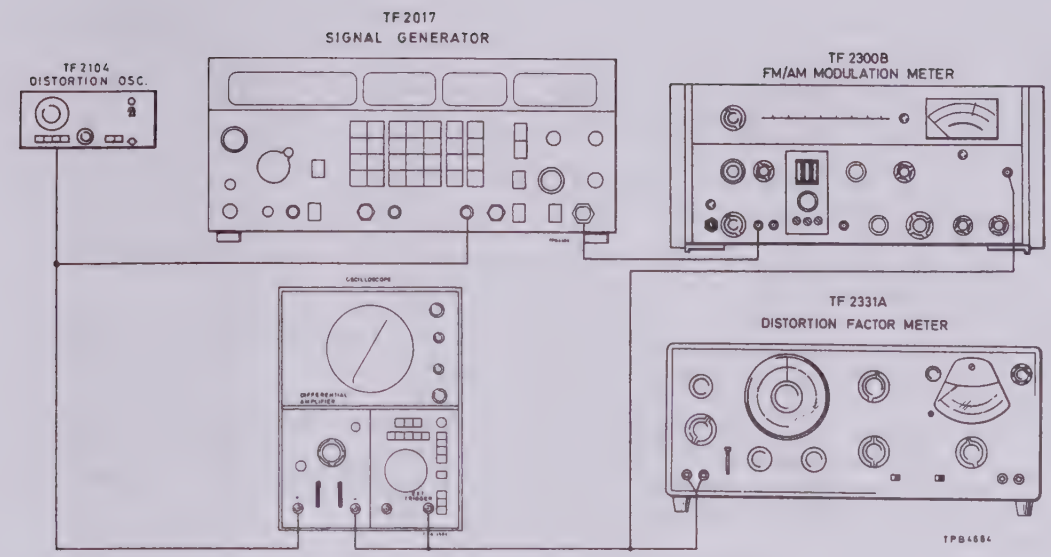


Fig. 14 Test gear arrangement for f.m. pre-distortion alignment (AS5)

(7) Again switch off the external a.f. source and check that the voltage at TP4 is still within 0.2 V of 24 V, if necessary re-adjust R2 and repeat the above procedure. Switch on the audio source again and increase the amplitude until the straight line trace shows signs of clipping i.e. a short tail on either end of the trace. This should occur at a measured f.m. deviation of about 230 - 240 kHz.

(8) With external modulation off, connect multimeter between TP5 and earth and adjust R13 for the same voltage as that measured at TP4 previously in step (6). Set the 2017 to FM OFF, connect the multimeter between TP4 and earth and adjust R12 for the identical value measured previously in step (6).

(9) Re-adjust the external d.c. source to +10 V if necessary and remove the external a.f. source. Set the 2017 to FM INT, 160 kHz DEVIATION, MODULATION OSCILLATOR to 1 kHz, FM ON. Check the modulation meter deviation and adjust R16 to give an average deviation reading of 160 kHz.

101. Select 2017 CARRIER FREQ to 256.1 MHz (unlock), FM DEVIATION of 2.5 MHz, FM INT, FM ON, check that the 2017 displays the correct carrier frequency.

(1) Reduce the variable d.c. external power set previously at +10 V to -1 V and adjust R15 for a change in the displayed carrier frequency of -500 kHz ±50 kHz.

(2) Increase the external d.c. to +21 V and check that the displayed carrier frequency is now +500 kHz ±50 kHz.

(3) Reset the FM DEVIATION to 160 kHz and check that the top head distortion is within specification at carrier frequencies of 16.1 MHz, 22 MHz and 32 MHz with sync volts at -1 V, +10 V and +21 V in each case. Also check that the f.m. deviation remains at 160 kHz ±4.25 kHz.

102. Select 2017 CARRIER FREQ to 256.1 MHz (unlock) INT FM OFF. Adjust the FINE TUNE control to give 0 V at TP6.

(1) Set external d.c. source to +10 V and note the 2017 displayed carrier frequency.

(2) Re-adjust the external d.c. source to +21 V and set R14 to give a 500 kHz increase in the carrier frequency.

(3) Re-adjust the external d.c. source to -1 V and set R20 to give a 500 kHz decrease in the carrier frequency.

(4) Reset 2017 CARRIER FREQ to 22 MHz (unlock) INT FM ON, MODULATION OSCILLATOR 1 kHz, FM DEVIATION 5 kHz. Carry out the following adjustments with external source volts at -1 V, +10 V and +21 V as shown below to obtain 5 kHz deviation in each case.

External d.c. source	*Adjust*	*Deviation*
+10 V	R18	5 kHz
+21 V	R19	
-1 V	R17	

Reset 2017 CARRIER FREQ first to 32 MHz (unlock) and then to 16.1 MHz (unlock) with an external d.c. source of +10 V. Re-adjust R18 for equal error about 5 kHz.

103. Remove the external d.c. source from SKBN and reconnect the 2017 fine freq. sync drive connection previously disconnected in para. 100. Set TP6 to 0 V by adjusting R13 on board AL4. Reset 2017 CARRIER FREQ to 256.1 MHz (unlock) FM DEVIATION to 2.5 MHz MODULATOR OSCILLATOR OFF. Switch FM ON and OFF noting any change in the carrier frequency, this should be less than 200 kHz.

Auto levelling circuit alignment (AA21)

104. The Amplitude Modulator board AA21 is supplied with an auto levelling error drive kit comprising D11/D13/R119. Each kit has a group number reference which is indicated on an adhesive label within the package. This label should be fixed on the board alongside the components if replacement is necessary. R86 is then adjusted according to Table 15 below to achieve the correct error drive.

TABLE 15 ERROR DRIVE SETTINGS

Diode group	*R119 value*	*Set current TP18/TP19 mA*	*Voltage mV TP21/earth*
13	27 kΩ	2.6	43
14	27 kΩ	2.4	39
15	27 kΩ	2.2	35
16	30 kΩ	2.1	34
17	33 kΩ	1.9	31
18	39 kΩ	1.7	28
19	47 kΩ	1.5	25
20	68 kΩ	1.2	20
21	82 kΩ	1.1	19
22	100 kΩ	1.0	18
23	110 kΩ	0.9	16
24	120 kΩ	0.7	12
25	130 kΩ	0.5	8

Pre-set and SIC components

105. The following table supplies details of the pre-set components and their function where possible; also included are the SIC components which normally do not require re-selection except in the event of repair or re-calibration. This should, whenever possible, be carried out by the Marconi Instruments' agent or Service Division. Each component location is identified where possible in Chap. 7 Component layout diagrams.

TABLE 16 PRE-SET & SIC COMPONENTS

Unit	*Circuit ref.*	*Location Chap.7,Fig.*	*Purpose*	*ADJ/ SIC*
AP1	R15	5a	Voltage r.f. sensor (adj. for 2.35 V d.c. at IC3 pin 10).	ADJ
	R51	5a	Sense voltage (monitor across C2, adj. for last trace to come on with a voltage input of 197 V).	ADJ
AP2	R1	5a	+5 V	ADJ
	R5	5a	+12 V } see para. 39 for details.	
	R12	5a	-5 V	
	R15	5a	Ripple null.	ADJ
	TR3/R22/R23	5a	3 part kit, supplied to give standardized low noise ref.	SIC
	R29/R30	5a	+70 V - see para. 39 for details.	SIC
AL4	R13	11a	Pre-distortion - see para.103 for details.	ADJ
	R19	11a	Sample & hold cct. short TP21 to earth and select R19 to give 2 mA current.	SIC
	R12	11a	First check R19 selection is correct then select UNLOCK mode of operation, adj. R13 and, if necessary select R12 for 10.0V ±0.1V at TP24.	ADJ/ SIC
	R13	11a		

TABLE 16 PRE-SET & SIC COMPONENTS (continued)

Unit	*Circuit ref.*	*Location Chap.7,Fig.*	*Purpose*	*ADJ/ SIC*
AL5	R19	12a	Apply i/p of 1MHz at SKAC, level 60mV and check for stable o/p at TP10.	SIC
AA21	R62	16a	Adj.for 4.6V ±0.05V at TP16 (set mod bias current).	ADJ
	R86	16a	Milliammeter across TP18/TP19 set to value shown in table.	ADJ
	R93	16a	Adj. for 6.7V ±0.5V (set flatness).	ADJ
	R121	16a	Set carrier freq. 75MHz Range 6, Mod on, full o/p, set R121 fully clockwise. Tune spectrum analyser to o/p signal (20kHz span). Set pulse mod off and rotate R121 until residual signal no longer decreases.	ADJ
	D11/D13/R119	16a	Auto levelling error drive, matched set (see para. 104 & Table 15).	SIC
	C43 C51 C52 C53	16a	Selected for best freq. response flat to within 4dB over the range 3.8MHz-1050MHz.	SIC
	R11	16a	Disconnect AA25 tag 6, select Range 9, remove mini-jump TP13/TP14. Connect d.v.m. between TP13 & earth, select R11 for +6V ±1V.	SIC
	R37	16a	Search osc. high VCO line.	SIC
AA23	R3	17a	Disconnect tag 3 external connection, connect 50µA meter between tag 3 and earth. Adj. R3 for 1µA.	ADJ
AA31	R97	18a	+10dB output stage, set level.	SIC
	R98/L42	18a	+10dB output stage, set level.	SIC
AB1	R3	20a	4-8MHz signal level.	ADJ
AB2	R56/R137	21a	Linear level controller.	ADJ
	R96	21a	+5dB gain, set for least carrier distortion.	ADJ
	R100	21a	TR26 constant current source, adj. for 200mA d.c.	ADJ
	R151	21a	ALC IC8 off-set null <1m, d.v.m. connections +ve to TP18, -ve to TP17.	ADJ
	R153	21a	ALC off-set balance control <3mV, d.v.m. connections +ve to TP3, -ve to TP19.	ADJ
	R159	21a	ALC IC9 off-set null <1mV, d.v.m. connections +ve to D15 cathode, -ve to TP16.	ADJ
	R213	21a	ALC IC12 off-set null <1mV, d.v.m. connections +ve to TP21, -ve to TP20.	ADJ

TABLE 16 PRE-SET & SIC COMPONENTS (continued)

Unit	*Circuit ref.*	*Location Chap.7, Fig.*	*Purpose*	*ADJ/ SIC*
AB2	C24, C31, C36, C45, C49	21a	HF response above 500MHz.	SIC
	R31, R32	21a	Connect d.v.m. 24V d.c. range between TP1 (+ve) and TP2 (-ve). Select carrier freq. in Range 1 band and select R32 for a reading of between 40-350mV. Select R31, if necessary, to ensure R32 remains within the values 1kΩ-10kΩ.	SIC
	R44	21a	Set for least carrier distortion.	SIC
	R73/R74/R75	21a	Level adj.	SIC
AS3	R1	26a	Fine level c.w. end } see para. 64	ADJ
	R2		Fine level c.c.w. end } for details	
	R3	26a	Connect probe tip to TP2 and probe earth to TP1. Select Ext mod, no signal input, adj. of 0V.	ADJ
	R4	26a	IC7 input off-set (unlevelled mode).	ADJ
	R5	26a	Adj. gain for 2V r.m.s. o/p with 1V r.m.s. i/p.	ADJ
	R6	26a	Input off-set voltage (levelled mode).	ADJ
	R7	26a	Mod level.	ADJ
	R8	26a	Output level calibration Ranges 2-9.	ADJ
	R9	26a	Range 1 level ref. (+126dBμV).	ADJ
	R10	26a	Range 1 +6dB level reference (+132dBμV).	ADJ
AS4	R25	27a	Audio gain.	ADJ
AS5	R1 to R20	28a	Adjustments should be carried out as described in the FM pre-distortion alignment procedure.	ADJ
	R128, R135	28a	Mimic detector compensation.	SIC
AK4B	R18	29a	Output level.	ADJ
AR1B	R9	31a	Set threshold level at TP1 for 0.8 V.	ADJ
AS7A	R5	33a	Master osc. current source, set for 10mA.	ADJ
	R9	33a	Low/$\overline{\text{High}}$ VCO geometric mean changeover. Increase Range 9 freq. manually until VCO changeover takes place, instruction can be monitored at AA21 pin 13. Adj. R9 so that the centre of the hysteresis occurs at 710 MHz.	ADJ

TABLE 16 PRE-SET & SIC COMPONENTS (continued)

Unit	*Circuit ref.*	*Location Chap.7,Fig.*	*Purpose*	*ADJ/ SIC*
AS7A	R16 to R19	33a	Selected in initial manufacture only	SIC
AS7B	R35	33a	Select motor drive and restrict movement from gear box assy., adjust R35 to give 570mV at TP1.	ADJ

Chapter 5, Annex A

MEASUREMENT OF PHASE NOISE IN SIGNAL GENERATORS

CONTENTS

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1 Side band noise
Reprint of article : 'Measurement of phase noise in signal generators'

Fig.
1 A typical phase noise plot for the TF 2020
2 Basic quadrature technique
3 Quadrature technique incorporating a p.l.l. to obtain phase quadrature at the mixer
4 Quadrature technique with a low noise pre-amplifier
5 FM discriminator method
6 An amplifier configuration
7 Residual phase noise characteristics

Side band noise

1. Side band noise measurements require the use of specialized equipment which is not always available to the user. Some methods of measuring side band noise are contained in this annex.

In recent years there has been considerable interest in the measurement of the phase characteristics of frequency sources. Two methods of measuring phase noise are presented, the quadrature and the f.m. discriminator methods. The calibration of each system is explained in terms of simple narrow band modulation theory and a minimum of mathematics is used throughout.

Measurement of phase noise in signal generators

D. P. Owen, B.Sc. (Hons)

All signal sources exhibit some degree of randomness in their frequency and amplitude due to the effects of random noise, interference, temperature fluctuations and other physical influences. For convenience these effects can be considered as being equivalent to a combination of amplitude modulation and angle modulation, i.e. phase or frequency. The amplitude modulation component is generally much less troublesome in signal generators since its magnitude is usually much smaller than the random angle modulation.

Over the years many methods of measuring random phase modulation have been used. For f.m. applications the most convenient measurement technique is to measure the equivalent f.m. deviation recovered by a low noise receiver tuned to the carrier frequency. The residual demodulated f.m. is measured in a specified audio band, or a weighted band such as that used for telephones, and represents the average peak f.m. deviation. Alternatively in phase modulation applications the equivalent residual phase modulation expressed in radians or degrees can be measured. As with f.m. measurement, the measurement is taken in a specified bandwidth and represents the average peak phase deviation, though occasionally the peak-to-peak value is quoted. These results, however, only give a limited idea of the characteristics of a generator and for many applications the single figure is not adequate. A more convenient method of defining phase noise modulation is to express the noise as the noise power contained in a single sideband in a 1 Hz bandwidth, at a specified offset frequency from the carrier, relative to the carrier power. If the noise at various frequency offsets is measured an s.s.b. noise plot such as that shown in Fig. 1 can be drawn. The ratio of phase noise power to carrier power is generally expressed as a logarithmic ratio and therefore has units of dBc/Hz, where dBc is decibels relative to carrier power.

In general, phase noise is highest at low offset frequencies and falls with increasing offset frequency until the amplifier noise floor is reached. The white noise added to the carrier signal by the amplifiers in the signal source effectively contributes equal amounts of phase and amplitude noise modulation and hence will contribute a phase noise power of −3 dB relative to the white noise power in a 1 Hz bandwidth. Provided that the total equivalent phase modulation (ph.m.) deviation is much less than 1 radian the phase noise plot may be used to derive an approximation to the residual ph.m. or f.m. deviation using a fairly simple if somewhat tedious algebraic routine.

For phase modulation the band of interest can be split in sub-bands of frequency each having roughly constant phase noise power. The total phase noise power, N, in a sub-band can then be calculated from the general formula

$$N_1 = N_A \log B_1 \text{ dBc}$$

where N_A is the average noise power/Hz in the sub-band of bandwidth B_1.

From this the equivalent ph.m. deviation in each band can be calculated by noting that narrow band modulation theory gives the result that 1 radian deviation gives a −6 dB carrier sideband. Hence if the noise in a given sub-band is −66 dB this is equivalent to a deviation of 0·001 radian (−60 dB relative to 1 radian). The total ph.m. deviation is then found by taking the square root of the sum of the squares of the deviations in each band.

The residual f.m. deviation can be found using the same technique but the sideband power in each sub-band is converted into an equivalent f.m. deviation using narrow band modulation theory. If the sub-band power is −66 dB and the average offset frequency of the sub-band is 1 kHz the equivalent f.m. deviation is 1 Hz, i.e. −60 dB relative to 1 kHz. Again the total f.m. deviation is found by taking the square root of the sum of the squares of the deviations in the sub-bands. This method will only give an approximate idea of the residual modulation but it can be a useful technique if the manufacturers information does not give the residual modulation in the required bandwidth.

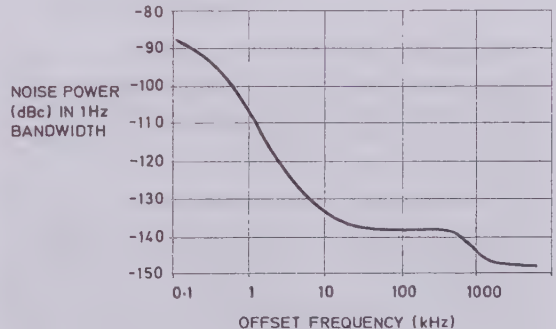

Fig. 1. A typical phase noise plot for the 50 kHz – 520 MHz Synthesized Signal Generator type TF 2020.

Measurement of phase noise

The most significant area of phase noise performance in signal generators is the phase noise at offset frequencies greater than 100 Hz from the carrier frequency and up to frequency offsets where the white noise of the amplifiers used contributes most of the noise. This amplifier noise floor should ideally be at least −140 dBc/Hz in a high quality signal generator and so any useful measurement system should have a residual noise floor of better than −150 dBc/Hz at offsets greater than 10 kHz.

It is technically not practical to measure this level of phase noise directly with a spectrum analyser because of the required dynamic range and so measurement techniques usually rely on first removing the carrier power.

There are two useful techniques for signal generator measurement – the quadrature and the f.m. discriminator method. Both of these systems rely on the availability of a reference source to effectively help to remove the carrier signal. In the following discussion it is assumed that the reference source contributes a negligible amount of phase noise to the signal generator. This is normally the case if a low noise crystal oscillator is used as the reference source.

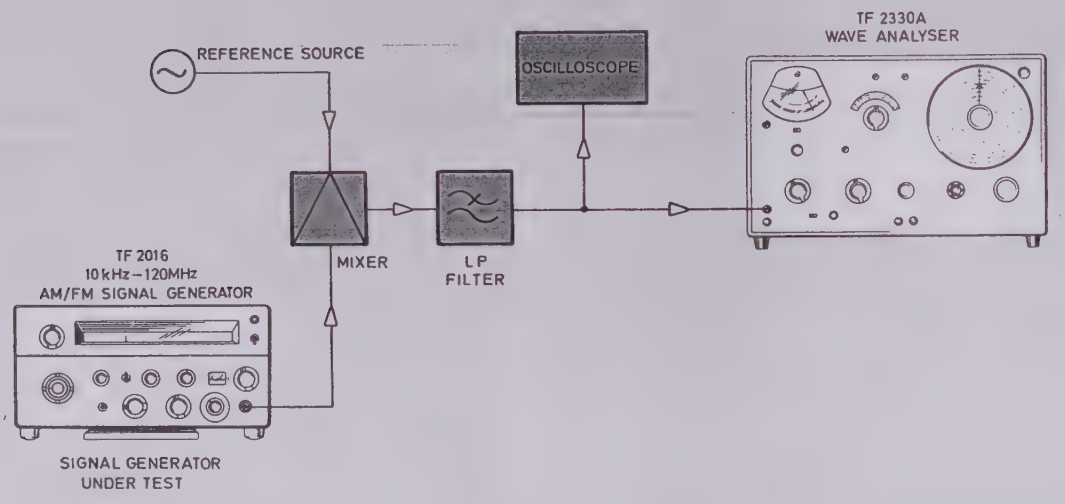

Fig. 2. Basic quadrature technique.

The quadrature technique

Fig. 2 shows the basic quadrature technique. The frequency source under test is mixed with a signal from a reference source in a double balanced mixer with a d.c. coupled output point. The output signal is then filtered to remove the high frequency signals from the mixer, amplified, if necessary, by an optional preamplifier and is then measured by a selective analyser such as a wave analyser or a spectrum analyser. The input frequencies to the mixer are adjusted such that the output from the mixer is a low frequency beat note. As the two frequencies are adjusted to be successively closer the output frequency from the mixer becomes lower until when the two frequencies are identical the output is just a d.c. level. If the two frequencies are in phase the d.c. level is a maximum and if they are in phase quadrature, i.e. 90° out of phase, the output level is approximately zero. The quadrature condition corresponds to the point at which the mixer is behaving as a phase detector since if the phase of one signal was changed by a small amount the d.c. level from the mixer would change. In a similar manner the in-phase condition corresponds to the mixer behaving as an amplitude detector. Clearly if the input signals are set to phase quadrature any phase noise on the signals would appear at the output of the mixer as a baseband noise signal and hence the selective analyser will measure a noise signal which is directly proportional to the phase noise of the source under test at an offset frequency corresponding to the frequency at which the selective analyser is set.

The system may be calibrated by offsetting the two input signals such that a beat note is generated at the output of the mixer. The r.m.s. beat note amplitude, V_B, is then measured by the selective analyser and this level is used as a reference level that is equivalent to a coherent phase sideband 6 dB below the carrier. This can be intuitively understood by noting that the peak voltage output from the mixer is equivalent to the phase sensitivity of the mixer at quadrature in radians/volt. Hence the beat note can be considered as corresponding to an equivalent narrow band phase modulation of 1 radian and narrow band modulation theory tells us that this is equivalent to a sideband level of −6 dB.

There are further correction factors which have to be taken into account for the selective analyser characteristics, which are dependent on the type of analyser used. If the TF 2330A Wave Analyser is used its bandwidth and detector characteristics must be accounted for. The detector uses an averaging technique which is calibrated to show the r.m.s. value of a sine wave. If the analyser is measuring a noise signal rather than a coherent sine wave it can be shown[1] that it is necessary to add 1·05 dB to the reading in order to

obtain the correct noise level. As the wave analyser noise bandwidth is approximately 7 Hz, it is necessary to weight the analyser reading to give the equivalent noise in a 1 Hz bandwidth. The wave analyser therefore gives a reading approximately 8·5 dB higher than the noise in a 1 Hz bandwidth. The meter indication on the wave analyser will exhibit a significant amount of jitter and so the meter indication has to be averaged visually or the meter movement has to be damped by adding capacitance in parallel. Alternatively a damped meter may be connected to the external monitor jack providing the constraints on loading the monitor are observed.

The TF 2370 Spectrum Analyser[2] may also be used as a tuned voltmeter. The noise bandwidth of the filter being used in the spectrum analyser should be checked if accurate noise measurements are required but generally the effective noise bandwidth of most analysers is approximately 15% greater than the 3 dB bandwidth of the filter. The correction factor for the bandwidth of the spectrum analyser is given by the general formula: $-10 \log B$
where B is the analyser noise bandwidth.

The detector correction factor for the 5, 50 and 500 Hz filters of the TF 2370 is the same as that for the wave analyser, i.e. +1·05 dB, provided that the analyser is used in the linear mode. If the analyser is used in the logarithmic mode the peaks of the noise waveform are effectively 'crushed' and the correction factor has to be changed to +2·5 dB.

TF 2370 should be used in the manual scan mode since in this mode a 1·5 Hz video filter is automatically incorporated. The frequency setting of the analyser may be manually scanned and a permanently stored display of the frequency characteristics of the phase noise sidebands is obtained. The internal frequency counter can also be used to accurately identify the frequency of any spurious signals that are present.

Summary of calibration factors

In the quadrature method the required calibration factors can be summarized as follows.

For a wave analyser or a spectrum analyser in the linear mode the phase noise, N, at the offset frequency, f_0, of the analyser is

$$N = -6 + 1{\cdot}05 - 10 \log B + 20 \log V_0/V_B \text{ dBc/Hz}$$

where B is the analyser noise bandwidth,

V_0 is the measured output voltage from the mixer at phase quadrature,

and V_B is the measured beat note amplitude.

For coherent sidebands it is not necessary to correct for the analyser characteristics and the phase sideband level is given by

$$N = -6 + 20 \log V_0/V_B \text{ dBc/Hz}$$

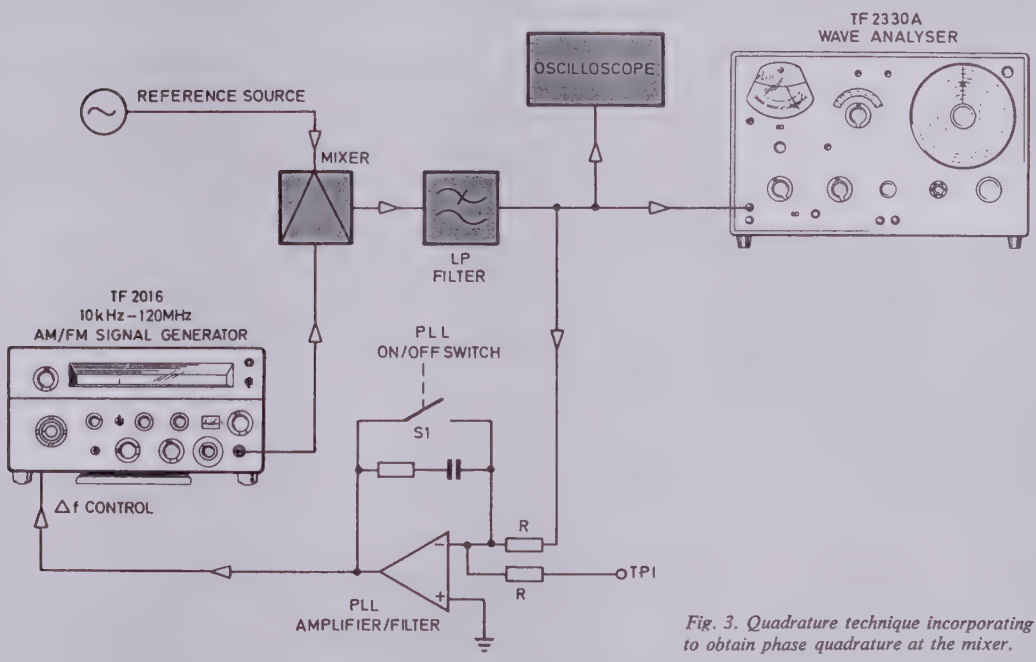

Fig. 3. Quadrature technique incorporating a p.l.l. to obtain phase quadrature at the mixer.

For a spectrum analyser in the logarithmic mode the phase noise is given by

$$N = -6 + 2{\cdot}5 - 10 \log B + 20 \log V_0/V_B \text{ dBc/Hz.}$$

Obtaining phase quadrature

The principal problem in using the quadrature technique for measurements on signal generators is to establish phase quadrature. Unless the generator has a synthesized frequency source it is unlikely that its frequency will remain in quadrature for a sufficient length of time for a measurement to be taken. If this is the case the only solution is to use a phase locked loop as shown in Fig. 3. The phase locked loop (p.l.l.) uses the electronic Δf control of the signal generator to control the output frequency of the generator. The phase locked loop bandwidth has to be designed to be significantly less than the lowest offset frequency at which the phase noise is to be measured since the loop will modify the in-band phase noise characteristics. The system is calibrated

by removing the phase lock and measuring the amplitude of the beat note as before.

When the system is phase locked the p.l.l. bandwidth can be checked by injecting a low level variable frequency at TP1 in Fig. 3 and varying the frequency of the source until the amplitude of the signal appearing on TP2 is within 3 dB of the signal level at TP2. This frequency will be approximately equal to the loop bandwidth and phase noise measurements should only be taken at frequencies at least an octave above this.

Quadrature measurement capability

The measurement capability of the system is determined by the beat note level recovered from the mixer and the noise and dynamic range of the selective analyser used. In most cases the resolution may be improved by using a low noise preamplifier to amplify the signal from the mixer as shown in Fig. 4. When the system is being calibrated the preamplifier is removed to prevent overloading the preamplifier and the selective analyser. When the noise is being measured the preamplifier is switched in and an oscilloscope is used to check that the maximum input level to the analyser is not exceeded and that phase quadrature has been set. The gain of the preamplifier has to be corrected for when calculating the measured phase noise.

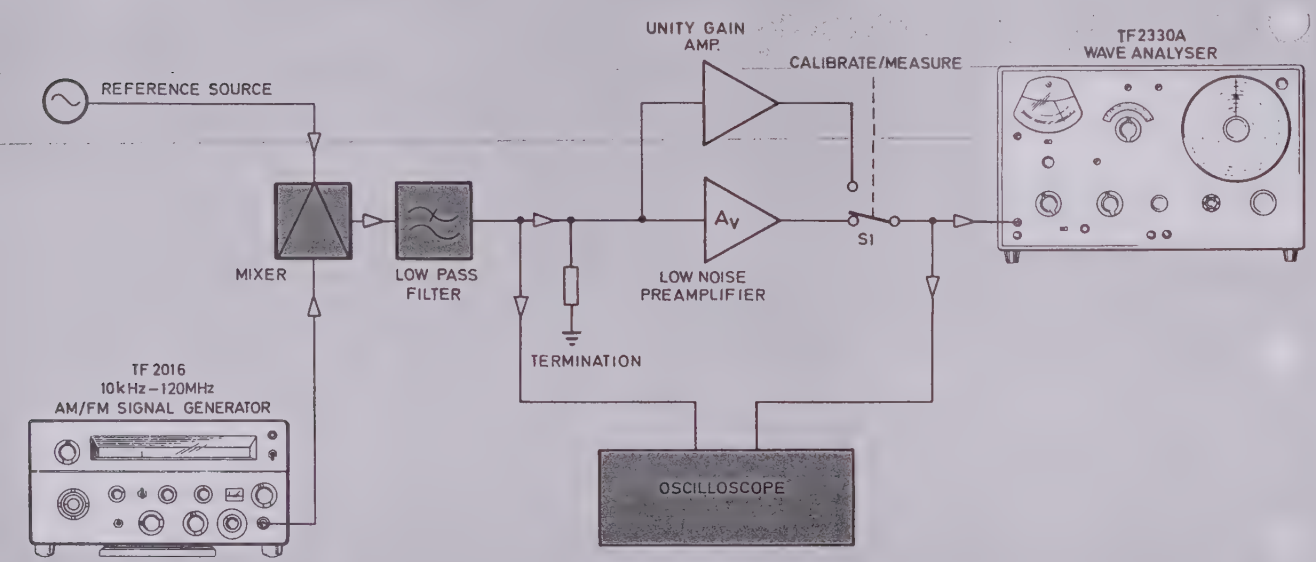

Fig. 4. Quadrature technique with a low noise preamplifier.

If the preamplifier has a gain sufficiently high so that the noise of the analyser has no effect on the system resolution the noise floor capability of the system can be estimated if the equivalent input noise voltage of the preamplifier is known and the amplitude of the beat note is measured. In practice the best discrete audio amplifiers will have an equivalent input noise voltage of approximately 2 nV/Hz at frequencies greater than 4 kHz which is roughly equivalent to the thermal noise of a 250 Ω resistor. For a recovered beat note of 30 mV r.m.s. the noise floor is then given by

$$N = -6 + 20 \log \frac{2 \times 10^{-9}}{30 \times 10^{-3}} = -149 \text{ dBc/Hz.}$$

Most common operational amplifiers have an input noise voltage of 15 nV/Hz so the system floor noise using one of these devices as a preamplifier would be around −132 dB/Hz. A low noise operational amplifier such as the TDA1034N with a typical performance of 3·5 nV/Hz would give a noise floor of around −144 dB/Hz. Clearly, increasing the drive level to the mixer will improve these results in proportion to the increased beat note derived from the mixer, provided that the reference source does not contribute any significant noise to the system.

The main drawbacks of the quadrature technique are that the signal sources have to be very stable, or a phase locked loop has to be used, and that the system calibration changes every time the recovered level from mixer is changed. There are methods of automating the measurements[3] but these techniques add significantly to the cost and the complexity of the system.

FM discriminator method

Marconi Instruments has used the f.m. discriminator technique shown in Fig. 5 for the last 7 years to check the phase noise characteristics of low noise signal generators. The outputs of the reference source and the signal generator are combined in a double balanced mixer to derive a nominal 1·5 MHz i.f. frequency. This is filtered to remove the unwanted components from the mixer and then amplified by a low noise amplifier before passing to a high gain limiting amplifier. This is followed by an f.m. discriminator that demodulates the spurious f.m. present in the 1·5 MHz i.f. The demodulated signal is then amplified and measured on a wave analyser.

The f.m. discriminator is designed such that it has a large change of output voltage with a small change of input frequency and has an f.m. bandwidth of 40 kHz. The high slope of the discriminator means that the i.f. frequency has to be tuned to within approximately 5 kHz of 1·5 MHz in order to remain in the linear portion of the discriminator characteristics. As an aid to this adjustment the tuned voltmeter that detects the i.f. level has a Q such that if the

signal generator frequency is tuned to obtain a peak reading on the i.f. voltmeter the i.f. frequency accuracy is adequate.

The calibration of the system is independent of the i.f. level recovered from the mixer since the limiter ensures that the drive level to the discriminator is always the same. Another advantage with this system is that when it is used for non-synthesized sources slow changes in the free running frequency of the generator will have no effect on the measurement accuracy provided that the drift is not sufficient to cause the l.f. frequency to drift outside the linear part of the discriminator characteristics.

When using the system it is important to realise that the demodulated output is the demodulated f.m. noise and not the phase noise and hence an additional correction factor is required which is dependent upon offset frequency.

The system is calibrated using a standardized f.m. source. With the amplifier gain set to unity the signal generator is replaced with an f.m. source modulated at 1 kHz to give 1 kHz deviation. The demodulated audio output is then

If coherent signals are being measured the formula is reduced to

$$N = -6 - A_V - 20 \log f_0/10^2 + 20 \log V_0/V_R \text{ dBc/Hz.}$$

In practice, the system only has to have an occasional calibration check since all the factors above are dependent upon the system characteristics and not the r.f. input level. A table of correction factors is provided on the front panel of the instrument which gives correction figures for various offset frequencies of interest. The correction factors include the wave analyser characteristics and hence the phase noise of the signal generator is given by adding the correction factor for the offset frequency being measured to the measured output voltage in dB referred to a fixed datum level.

The input level to the wave analyser is monitored by an oscilloscope in order to ensure that the wave analyser is not overloaded. In this respect, however, the system has a further advantage over the quadrature technique. The lower

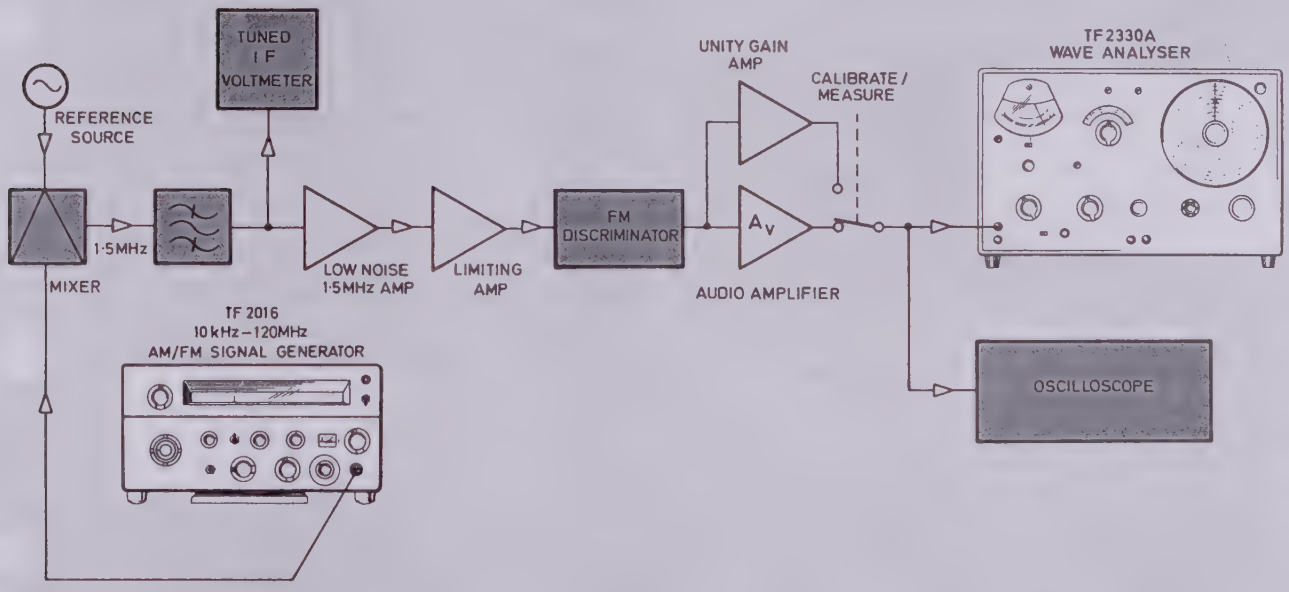

Fig. 5. FM discriminator method.

measured by the wave analyser. This level is again equivalent to a phase sideband at −6 dB. As in the quadrature method if a TF 2330A Wave Analyser is used there is a correction factor of +1·05 dB for the detector and −8·5 dB for the analyser bandwidth. In addition there is another correction factor dependent on the offset frequency being measured. The discriminator effectively has a linearly increasing phase gain as the offset frequency is increased. Hence the phase noise is given by the expression

$$N = -6 + 1{\cdot}05 - 10 \log B - A_V - 20 \log f_0/10^3 + 20 \log V_0/V_R \text{ dBc/Hz.}$$

where B is the noise bandwidth of the wave analyser,

A_V is the audio preamplifier gain,

f_0 is the offset frequency at which the noise is being measured,

V_0 is the measured output noise voltage,

and V_R is the output voltage measured in the calibration described previously.

frequency phase noise sidebands are not amplified as much as the high frequency components, by the discriminator, and hence the dynamic range required in the analyser is less. This can be an important advantage when measuring the characteristics of valve generators. Such sources frequently have very good phase noise characteristics at a 20 kHz offset but can have strong mains hum and low frequency phase noise components which could overload the measurement system.

If required, the output of the discriminator can be converted to be directly proportional to phase noise, as opposed to frequency noise, by using a suitable amplifier as shown in Fig. 6.

Measurement capability

The system noise floor of a discriminator system in use at Marconi Instruments is shown in Fig. 7 for a recovered i.f. level of 30 mV. The floor noise at 20 kHz offset is −153 dB and is due to the noise generated at the input to the 1·5 MHz amplifier. This low noise floor is fairly easily

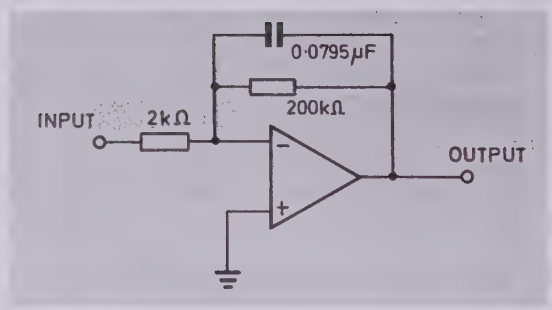

Fig. 6. An amplifier configuration capable of converting f.m. noise into phase noise. The gain at the calibration frequency of 1 kHz is unity and its lower 3 dB bandwidth is 10 Hz.

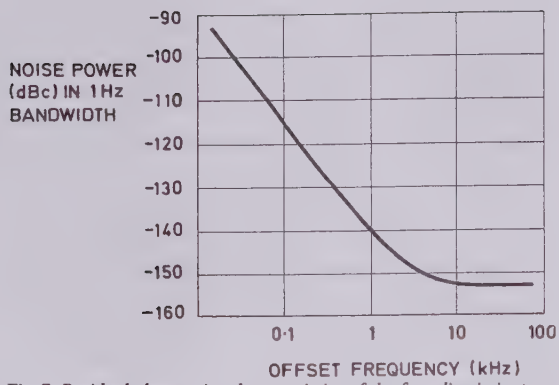

Fig. 7. Residual phase noise characteristics of the f.m. discriminator system used for a recovered i.f. level of 30 mV r.m.s. This was measured at r.f. input frequencies of 10 and 11·5 MHz, 140 and 141·5 MHz and 420 and 421·5 MHz using low noise crystal oscillators.

achieved since transformer techniques can be used to optimize the operating conditions of the amplifier. The audio amplifier after the discriminator is driven from a 100 kΩ source impedance, which is the output impedance of the discriminator, and as a result a j.f.e.t. source follower followed by an operational amplifier, such as the μA 741, is perfectly adequate for recovering the output signal. The high gain of the discriminator ensures that the noise performance of the amplifier is not critical.

The noise floor at 20 kHz is directly dependent upon the i.f. level but below 1 kHz it is independent of i.f. level for levels greater than 15 mV. Its source is believed to be in either the discriminator or the limiters but so far no attempt has been made to minimize it since the noise floor is more than adequate for signal generator applications.

The principal limitation on the technique is that the offset frequency that can be measured is limited to 40 kHz by the f.m. bandwidth of the discriminator. However, in many applications this does not reduce the usefulness of the system.

References

1. BRODERICK, P.: 'Noise measurements with electronic voltmeters'; *Marconi Instrumentation*, August 1965, **10**, p.18.

2. MIDDLETON, J. D. et al: '110 MHz Spectrum Analyser'; *Marconi Instrumentation*, December 1973, **14**, p.50.

3. LANCE, A. L. et al: 'Automated phase noise measurements'; *Microwave Journal*, June 1977, **20**, No. 6, p.87.

Printed in Great Britain by Albert Frost & Sons Ltd, Rugby

Chapter 6

REPLACEABLE PARTS

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9 Unit AK2 - Keyboard 1 and indicators
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12 Unit AP2 - Voltage stabilizers
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INTRODUCTION

1. Each sub-assembly or printed circuit board in this instrument has been allocated a unit identification, e.g. A0, AA11, AB2 etc.

2. The complete component reference carries its unit number as a prefix, e.g. AB2C3 (capacitor C3 on board AB2) but for convenience in the text and on circuit diagrams the prefix is not used. However, when ordering replacements or in correspondence the complete component reference must be quoted.

ABBREVIATIONS

3. The components are listed in alphanumerical order of the complete circuit reference and the following abbreviations are used :

C	:	capacitor	R	:	resistor
Carb	:	carbon	S	:	switch
Cer	:	ceramic	SK	:	socket
Con assy	:	connector assembly	T	:	transformer
CSR	:	controlled silicon rectifier	Tant	:	tantalum
D	:	semiconductor diode	TP	:	terminal
Elec	:	electrolytic	TR	:	transistor
FS	:	fuse	Var	:	variable
IC	:	integrated circuit (package)	W	:	watts at 70°C
L	:	inductor	WW	:	wirewound
LP	:	lamp	X	:	miscellaneous item
Max	:	maximum	†	:	value selected during test; nominal value listed
ME	:	meter			
Met	:	metal	⌀	:	feedthrough component
Mic	:	mica	⚠	:	static sensitive device } See Notes
Min	:	minimum	⚠	:	Beryllia, health hazard } & Cautions
Ox	:	oxide			
Pl	:	plug			
Plas	:	plastic			

COMPONENT VALUES

4. One or more of the components fitted in this instrument may differ from those listed in this chapter for any of the following reasons :

(a) Components indicated by a † have their values selected during test to achieve particular performance limits.

(b) Owing to supply difficulties, components of different value or type may be substituted provided the overall performance of the instrument is maintained.

(c) Numerous capacitor and inductor circuit references not included in this chapter are made up of stray capacitance or inductance inherent in a circuit. Where feasible a theoretical value has been calculated and the component shown with a circuit reference on the Servicing Diagrams, Chap. 7. Additionally, other capacitors and inductors are manufactured as part of the printed circuit board legend and therefore not included as replaceable parts.

(d) As part of a policy of continuous development, components may be changed in value or type to obtain detail improvements in performance.

5. When there is a difference between the component fitted and the one listed, always use as a replacement the same type and value as found in the instrument.

ORDERING

6. When ordering replacements, address the order to our Service Division (address on rear cover) or nearest agent and specify the following for each component required :

(1) Type* and serial number of instrument

(2) Complete circuit reference

(3) Description

(4) Marconi Instruments code no.

*As given on the serial number label at the rear of the instrument; if this is superseded by a model number label, quote the model number instead of the type number.

Circuit reference	Description	Code no.
	ELECTRICAL COMPONENTS	
	7. Unit A0 - Chassis	
C1	Elec 15 000µF -10+50% 16V	26426-097K
C2	Elec 15 000µF -10+50% 16V	26426-097K
C6	Elec 100µF -20+50% 100V	26415-816L
C7	Elec 220µF -20+100% 100V	26415-841A
C8	Elec 4700µF -10+50% 16V	26426-091P
C9	Elec 4700µF -10+50% 25V	26426-092X
C10	Elec 2200µF -10+50% 40V	26426-086D
C11	Elec 4700µF -10+50% 25V	26426-092X
C12	Tant 22µF 20% 15V	26486-230B
C13	Tant 47µF 20% 6V	26486-232A
C14	Tant 4.7µF 20% 35V	26486-219P
C15	Tant 22µF 20% 15V	26486-230B
CB1	Thermal circuit breaker 2-5700-L-2.5A	23488-602R
CB2	Thermal circuit breaker 2-5700-L-2.5A	23488-602R
Con/assy	For details see PL & SK connector assemblies	
D1	BY260-200 Rectifier bridge	28359-190S
D2	BY260-200 Rectifier bridge	28359-190S
LP1	12V 0.1A	23735-461Y
M1	Fan RL9-18/00	23535-106N

Circuit reference	Description	Code no.
	Fan seal	37490-493V
	Air filter	37490-431W
	Anti-vibration mount	22773-580H
PLAP	Connector/mains filter	23423-150L
PLAU	Con. assy. (PLAU-SKDP)	43129-496H
PLAV	Con. assy. (PLAV-PLCZ)	43129-497E
PLAW	Con. assy. (PLAW-SKDK)	43129-495Z
PLBN	Con. assy. (Fine freq. control)	43129-499Y
PLCF	Con. assy. (PLCF-SKDA)	43129-500A
PLCH	Con. assy. (PLCH-PLDT)	43129-503E
PLCM, PLCN	Con. assy. (PLCM-PLCN)	43129-501Z
PLCR, PLCT	Con. assy. (PLCR-PLCT)	43129-502H
PLCZ	Con. assy. (PLCZ-PLAV)	43129-497E
PLDD, PLDE	Con. assy. (PLDD-PLDE)	43129-498U
PLDT	Con. assy. (PLDT-PLCH)	43129-503E
R1	Var cermet multiturn 1kΩ 1W	25748-499T
R2	Var cermet log 1kΩ 10% 2W	25737-001G
R3	Var cermet 10kΩ 10% 2W	25725-404L
R4	Met film 470Ω 2% ¼W	24773-265M
R5	Var cermet 1kΩ 10% 2W	25725-460K

7. Unit A0 - Chassis (continued)

Circuit reference	Description	Code no.
SAX	3 PDT (FM-INT-EXT)	23462-263F
SAY	3 PDT (AM-INT-EXT)	23462-263F
SBC	SPDT (STD-INT-EXT)	23462-252Z
SBD	(COARSE LEVEL)	44340-143F
SBE	(FREQ. RANGE)	44340-144G
SBF	SPDT (COUNTER RES.)	23462-254E
SBH	(RF LEVEL UNITS)	44340-145V
SBJ	DPDT (LEVELLED-UNLEVELLED)	23462-258L
SE	DPST (SUPPLY-ON)	23465-410R
SKS	Con. assy.	43129-516W
SKT	Con. assy.	43129-515S
SKU	Con. assy. (SKU-SKDR)	43129-511J
SKAD	Con. assy.	43129-585T
SKAE	Con. assy	43129-581V
SKAF	Housing	23435-167C
SKAH	Con. assy	43129-534H
SKAJ	Housing	23435-993R
SKAK	Mains selector 115V	43169-024F
SKAK	Mains selector 230V	43169-025G
SKAL	Con. assy.	43129-584D
SKAM	Con. assy.	43129-582S
SKAN	Con. assy. (SKAN-SKBM)	43129-514V
SKAR	Housing	23435-988M
SKAT	Con. assy	43129-605E
SKAX	Con. assy. (SKAX-SKBL)	43129-673U
SKAY	Con. assy.	43129-510L
SKAZ	Con. assy.	43129-674Y
SKBA	Con. assy.	43129-512F
SKBE	Con. assy.	43129-676L
SKBF	Con. assy. (SKBF-SKBW)	43129-533Z
SKBH	Con. assy.	43129-535E
SKBJ	Con. assy.	43129-583W
SKBK	14-way	23435-142A
SKBL	Con. assy. (SKBL-SKAX)	43129-673U
SKBM	Con. assy. (SKBM-SKAN)	43129-514V
SKBP	Con. assy.	43129-675N
SKBU	Con. assy. (SKBU-SKDH)	43129-513G
SKBV	Con. assy.	43129-677J
SKBW	Con. assy. (SKBW-SKBF)	43129-533Z
SKCV	10-way	23435-044U
SKDA	Con. assy. (SKDA-PLCF)	43129-500A
SKDH	Con. assy. (SKDH-SKBU)	43129-513G
SKDK	Con. assy. (SKDK-PLAW)	43129-495Z
SKDL	BNC 50Ω Bulkhead type	23443-446H
SKDM	BNC 50Ω Bulkhead type	23443-446H
SKDN	BNC 50Ω Bulkhead type	23443-446H
SKDP	Con. assy. (SKDP-PLAU)	43129-496H
SKDR	Con. assy. (SKDR-SKU)	43129-511J
SKDU	16-way	23435-143Z

Circuit reference	Description	Code no.
	7. Unit A0 - Chassis (continued)	
SKDV	Con. assy.	43129-538N
SKDW	BNC 50Ω Bulkhead type	23443-446H
SKDX	BNC 50Ω Bulkhead	23443-446H
T1	Torroidal	43490-071B
T2	Mains	43490-072K
	8. Unit AK1 - Main keyboard	
	Complete board	44828-350L
D1 to D72	Diode 1N4148	28336-676J
R1 to R12	Met film 10kΩ 2% ¼W	24773-297M
SH to SAN	Switch Digitast type SREU ITT	23465-411B
	9. Unit AK2 - Keyboard 1 and indicators	
	Complete board	44828-351J
C1	Cer 0.01μF -20+80% 100V	26383-055L
D1 to D11	LED (Red LLL7)	28624-105D
IC1	7442	28465-003D
R1 to R9	Met film 240Ω 2% ¼W	24773-258D
R10	Met film 15kΩ 2% ¼W	24773-301P
SAP	Switch Digitast type SREU ITT	23465-411B
SAR	Switch Digitast type SREU ITT	23465-411B
TR1	BC239C	28452-771P
	10. Unit AK3 - Keyboard 2	
	Complete board	44828-351J
SAS SAT SAU SAV SAW	Switch Digitast type SREU ITT	23465-411B
	11. Unit AP1 - AC pre-regulator and mains selector	
	Complete board	44828-569C
C1	Cer 0.001μF 10% 63V	26383-585M

Circuit reference	Description	Code no.
	11. Unit AP1 - AC pre-regulator and mains selector (continued)	
C2	Tant 4.7µF 20% 35V	26486-219P
C3	Elec 1000µF -20+100% 16V	26415-825W
C4	Tant 4.7µF 20% 35V	26486-219P
C5	Tant 4.7µF 20% 35V	26486-219P
C6	Elec 220µF -20+100% 10V	26415-817J
C7	Cer 0.1µF -20+80% 30V	26383-031S
C8	Cer 0.1µF -20+80% 30V	26383-031S
C9	Tant 10µF 20% 35V	26486-225C
C10	Tant 15µF 20% 15V	26486-227B
C11 to C20	Cer 0.047µF 10% 50V	26343-560M
C21 to C30	Plas 0.01µF 20% 630V	26531-113G
C31	Cer 100pF 2% 63V	26343-477V
C32	Plas 0.1µF 10% 100V	26582-211B
C33	Cer 22pF 5% 63V	26343-469N
C34	Tant 10µF 20% 35V	26486-225C
C35	Cer 0.01µF -20+100% 40V	26387-253M
C36	Cer 0.01µF -20+100% 40V	26387-253M
C37	Cer 0.0047µF 10% 63V	26383-591B
CSR1 to CSR10	Triac TAG 425-800	28385-720N
D1	1N5401	28355-723N
D2	1N5401	28355-723N
D3 to D7	1N4004	28357-028K
D8	Z5B 7.5	28371-603H
IC1	µA7805	28461-707G
IC2	ZN404	28461-922T
IC3	67788 Gould Advance	28469-406E
IC4	ULN2001N	28461-921D
IC5	ULN2001N	28461-921D
L1	Choke 1mH	44290-850R
R1	Met film 330Ω 2% ¼W	24773-261D
R2	Met film 6.8kΩ 2% ¼W	24773-293D
R3	Met film 330Ω 2% ¼W	24773-261D
R4	Met film 6.8kΩ 2% ¼W	24773-293D
R5	Met film 100Ω 2% ¼W	24773-249J
R6	Met film 4.7kΩ 2% ¼W	24773-289W
R7	Met film 4.7kΩ 2% ¼W	24773-289W
R8	Met film 10kΩ 2% ¼W	24773-297M
R9	Met film 180kΩ 2% ¼W	24773-327W
R10	Met film 33kΩ 2% ¼W	24773-309Z
R11	Met film 33kΩ 2% ¼W	24773-309Z
R12	Met film 100kΩ 2% ¼W	24773-321L
R13	Met film 100kΩ 2% ¼W	24773-321L
R14	Met film 120Ω 2% ¼W	24773-251L
R15	Var cermet 100Ω 10% ½W	25711-635L

Circuit reference	Description	Code no.
	11. Unit AP1 - AC pre-regulator and mains selector (continued)	
R16	Met film 390Ω 2% ¼W	24773-263P
R17	Met film 39kΩ 2% ¼W	24773-311A
R18	Met film 330kΩ 2% ¼W	24773-333P
R19	Met film 10kΩ 2% ¼W	24773-297M
R20	Met film 10kΩ 2% ¼W	24773-297M
R21 to R30	Met film 33Ω 2% ¼W	24773-037S
R31 to R40	Met film 120Ω 2% ¼W	24773-251L
R41 to R50	Carb 1kΩ 10% ½W	24343-991W
R51	Var cermet 20kΩ 10% ½W	25711-642V
R52	Met ox varistor	25685-502H
R53	Met film 47kΩ 2% ¼W	24773-313H
SK	DIL 16-way	28488-041E
SK	DIL 28-way	28488-045L
TR1	BCY71	28435-235L
TR2	BCY71	28435-235L
TR3	BC239C	28452-771P
TR4	BC239C	28452-771P

Circuit reference	Description	Code no.
	12. Unit AP2 - Voltage stabilizers	
	Complete board	44828-342H
C1 to C6	Tant 4.7μF 20% 35V	26486-219P
C7	Cer 47pF 5% 63V	26343-473L
C8	Tant 4.7μF 20% 35V	26486-219P
C9	Elec 10μF -20%+50% 100V	26415-803R
C10	Elec 10μF -20+50% 100V	26415-803R
C11	Tant 10μF 20% 35V	26486-225C
C12	Tant 4.7μF 20% 35V	26486-219C
C13	Tant 4.7μF 20% 35V	26486-219C
C14	Tant 4.7μF 20% 35V	26486-219C
D1 to D4	1N5401	28355-723N
D5 to D21	1N4004	28357-028K
D22	LED (Red LLL7)	28624-105D
D23	1N4004	28357-028K
D24	1N4004	28357-028K
D25	LED (Red LLL7)	28624-105D
D26	1N825	28371-494Z

12. Unit AP2 - Voltage stabilizers (continued)

Circuit reference	Description	Code no.
D27	1N4004	28357-028K
D28	LED (Red LLL7)	28624-105D
D29	1N4004	28357-028K
D30	LED (Red LLL7)	28624-105D
D31	1N4004	28357-028K
D32	LED (Red LLL7)	28624-105D
D33	Z5B20	28372-786A
D34	Z5B20	28372-786A
D35	Z5B20	28372-786A
IC1	μA7824	28461-710G
IC2	μA7912	28461-718M
IC3	μA7905	28461-717X
IC4	NE 5534AH	28461-329V
IC5	LAS19U	28461-721M
IC6	LM 350K	28461-722C
R1	Var cermet 1kΩ 10% ½W	25711-638G
R2	Met film 510Ω 2% ¼W	24773-266C
R3	Met film 270Ω 2% ¼W	24773-259T
R4	Met film 2.2kΩ 2% ¼W	24773-281Y
R5	Var cermet 500Ω 10% ½W	25711-637F
R6	Met film 1.5kΩ 2% ¼W	24773-277U
R7	Met film 510Ω 2% ¼W	24773-266C
R8	Met film 680Ω 2% ¼W	24773-269K
R9	Met film 3kΩ 2% ¼W	24773-284J
R10	Met film 1.5kΩ 2% ¼W	24773-277U
R11	Met film 300Ω 2% ¼W	24773-260W
R12	Var cermet 50Ω 10% ½W	25711-634N
R13	Met film 510Ω 2% ¼W	24773-266C
R14	Met film 18kΩ 2% ¼W	24773-303M
R15	Var cermet 1kΩ 10% ½W	25711-638G
R16	Met film 10kΩ 2% ¼W	24773-297M
R17	Met film 2.2kΩ 2% ¼W	24773-281Y
R18	Met film 220Ω 2% ¼W	24773-257W
R19	Met film 18Ω 2% ¼W	24773-231P
R20	Met film 2.2kΩ 2% ¼W	24773-281Y
R21	Met film 2.2kΩ 2% ¼W	24773-281Y
R22, R23	† Part of FET kit for TR3	46883-258T
R24	Carb film 10MΩ 10% 1/8W	24321-885W
R25 to R28	Met film 82kΩ 2% ¼W	24773-319J
R29 †	Met film 1.6kΩ 2% ¼W	24773-278Y
R30 †	Met film 6.8kΩ 2% ¼W	24773-293D
R31	Met film 2.4kΩ 2% ¼W	24773-282N
R32	Met film 3.6kΩ 2% ¼W	24773-286G
R33	Met film 1.8kΩ 2% ¼W	24773-279N
R34	Met film 10kΩ 2% ¼W	24773-297M

Circuit reference	Description	Code no.
	12. Unit AP2 - Voltage stabilizers (continued)	
TR1	BF338	28458-577X
TR2	BFY51	28455-827T
TR3 †	BF244B (kit for TR3 including R22 and R23)	46883-258T
	13. Unit AL0 - Logic processor	
C1Ø to C12Ø	10pF ±1pF 300V	26333-228E
L1 to L6	0.33µH ±10%	23642-546U
PLC	Con. assy.	43129-518T
PLD	Con. assy.	43129-518T
PLE	Con. assy.	43129-518T
PLH	Con. assy.	43129-519P
PLJ	Con. assy.	43129-519P
PLK	Con. assy.	43129-517D
PLL	Con. assy.	43129-517D
PLN	Con. assy.	43129-517D
PLP	Con. assy.	43129-517D
PLW	Con. assy. (PLW-SKDE)	43129-506N
PLX	Con. assy.	43129-523X
PLY	Con. assy.	43129-523X
PLZ	Con. assy.	43129-568U
PLAA	Con. assy. (PLAA-SKAU)	43129-506N
PLAB	Con. assy. (PLAB-SKAV)	43129-507L
PLAC	Con. assy. (PLAC-SKAW)	43129-507L
SKM	Con. assy.	43129-551W
SKV	Con. assy	43129-552D
X1 to X4	Filter (Multi-section)	26397-301E
	14. Unit AL1 - Display	
	Complete board	44828-324W
D1 to D37	LED (Red HLMP0301)	28624-118Z
IC1	HP 5082-7616	28624-218K
IC2 to IC13	HP 5082-7611	28624-217B
IC14	HP 5082-7616	28624-218K
IC15	HP 5082-7611	28624-217B
IC16	HP 5082-7611	28624-217B
IC17	HP 5082-7611	28624-217B

Circuit reference	Description	Code no.
	14. Unit AL1 - Display (continued)	
R1 to R18	Met film 360Ω 2% ¼W	24773-262T
SK	DIP 14-way	28488-033B
SKA	Edge connector	23435-147Y
SKB	Edge connector	23435-147Y
	15. Unit AL2 - Display drive	
	Complete board	44828-325D
C1 to C19	Cer 0.001μF 10% 63V	26383-585M
C20	Elec 100μF -20+100% 25V	26415-813U
C21	Cer 0.001μF 10% 63V	26383-585M
C22	Elec 100μF -20+100% 25V	26415-813U
C23 to C32	Cer 0.001μF 10% 63V	26383-585M
D1	FH1100	28349-005Z
IC1	74LS164	28467-515G
IC2	7406	28469-158A
IC3	7406	28469-158A
IC4	74LS75	28462-408U
IC5	74LS00	28466-345H
IC6	74LS04	28469-171L
IC7	74LS47	28465-020H
IC8	74LS75	28462-408U
IC9	74LS02	28466-214Y
IC10	74LS47	28465-020H
IC11	74LS75	28462-408U
IC12	74LS47	28465-020H
IC13	74LS75	28462-408U
IC14	74LS42	28465-019U
IC15	74LS00	28466-345H
IC16	74LS47	28465-020H
IC17	74LS75	28462-408U
IC18	74LS47	28465-020H
IC19	74LS75	28462-408U
IC20	74LS02	28466-214Y
IC21	74LS47	28465-020H
IC22	74LS75	28462-408U
IC23	74LS47	28465-020H
IC24	74LS75	28462-408U
IC25	74LS164	28467-515G
IC26	7406	28469-158A
IC27	74LS47	28465-020H
IC28	74LS75	28462-408U

15. Unit AL2 - Display drive (continued)

Circuit reference	Description	Code no.
IC29	74LS164	28467-515G
IC30	7406	28469-158A
IC31	7406	28469-158A
IC32	74LS00	28466-345H
IC33	74LS00	28466-345H
IC34	74LS164	28467-515G
IC35	7406	28469-158A
IC36	74LS02	28466-214Y
IC37	74LS04	28469-171L
IC38	7403A	28466-322J
IC39	74LS47	28465-020H
IC40	74LS75	28462-408U
IC41	74LS47	28465-020H
IC42	74LS75	28462-408U
IC43	74LS47	28465-020H
IC44	74LS75	28462-408U
IC45	74LS47	28465-020H
IC46	74LS75	28462-408U
IC47	74LS75	28462-408U
IC48	74LS00	28466-345H
IC49	74LS47	28465-020H
IC50	74LS75	28462-408U
IC51	74LS04	28469-171L
IC52	74LS42	28465-019U
IC53	74LS47	28465-020H
IC54	74LS75	28462-408U
IC55	74LS47	28465-020H
IC56	74LS75	28462-408U
IC57	74LS164	28467-515G
IC58	7406	28469-158A
R1	Met film 360Ω 2% ¼W	24773-262T
R2	Met film 360Ω 2% ¼W	24773-262T
R3	Met film 510Ω 2% ¼W	24773-266C
R4 to R19	Resistor network 1kΩ 5%	24681-516B
R53	Met film 10kΩ 2% ¼W	24773-297M
R60	Met film 1kΩ 2% ¼W	24773-273A
R62 to R65	Met film 360Ω 2% ¼W	24773-262T
R66	Met film 1kΩ 2% ¼W	24773-273A
R74	Met film 2.2kΩ 2% ¼W	24773-281Y
R75	Met film 2.2kΩ 2% ¼W	24773-281Y
R82	Met film 1kΩ 2% ¼W	24773-273A
R84	Met film 10kΩ 2% ¼W	24773-297M
R91	Met film 1kΩ 2% ¼W	24773-273A

Circuit reference	Description	Code no.
	15. Unit AL2 - Display drive (continued)	
R93 to R96	Met film 360Ω 2% ¼W	24773-262T
R104	Met film 10kΩ 2% ¼W	24773-297M
R112 to R115	Met film 360Ω 2% ¼W	24773-262T
R116	Met film 1kΩ 2% ¼W	24773-273A
R117	Met film 510Ω 2% ¼W	24773-266C
R124	Met film 1kΩ 2% ¼W	24773-273A
R132	Met film 1kΩ 2% ¼W	24773-273A
R134	Met film 10kΩ 2% ¼W	24773-297M
R141	Met film 1kΩ 2% ¼W	24773-273A
R143 to R147	Met film 360Ω 2% ¼W	24773-262T
R148	Met film 10kΩ 2% ¼W	24773-297M
	16. Unit AL3 - Microprocessor system	
	Complete board	44828-326T
C1 to C7	Cer 0.01μF -20+100% 40V	26387-253M
C8	Tant 4.7μF 20% 35V	26486-219P
C9 to C16	Cer 0.01μF -20+100% 40V	26387-253M
C18	Cer 0.01μF -20+100% 40V	26387-253M
C19	Cer 0.01μF -20+100% 40V	26387-253M
C20	Tant 47μF 20% 6V	26486-232A
C22	Cer 0.01μF -20+100% 40V	26387-253M
C23	Tant 22μF 20% 15V	26486-230B
C24	Cer 4.7pF ±0.5pF 63V	26343-461B
C25	Cer 4.7pF ±0.5pF 63V	26343-461B
D1	1N4148	28336-676J
IC1	74S03	28466-353L
IC2	74S04	28469-177W
IC3	74S03	28466-353L
IC4	74LS04	28469-171L
IC5	74LS245	28469-188B
IC6 ⚠	D8291	28467-001F
IC7 ⚠	P8155	28469-304E
IC8 ⚠	P8085A	28469-396K
IC9	74LS74	28462-611A
IC10	74LS377	28462-619J
IC11	P8205	28465-030F
IC15 ⚠	P8155	28469-304E
IC16	74LS02	28466-214Y
IC17	74LS32	28466-108U

Circuit reference	Description	Code no.
	16. Unit AL3 - Microprocessor system (continued)	
IC21 ⚠	EPROM B1702AL2	44533-013G
	Note ... IC21 is individually programmed to the requirements of the Master Oscillator AS1 and is supplied as an integral part of the same.	
R1 to R6	Met film 10kΩ 2% ¼W	24773-297M
R7	Met film 47kΩ 2% ¼W	24773-313H
R8 to R13	Met film 10kΩ 2% ¼W	24773-297M
SK	(Mini jump shorting socket)	23435-990X
SK	DIL 24-way	28488-044N
SK	DIL 40-way	28488-046J
X1	Crystal 6.144 MHz	28312-054J
	17. Unit AL4 - Synchronizer/Counter 'B'	
	Complete board	44828-327P
C1	Cer 0.01μF -20+80% 100V	26383-055L
C2	Tant 4.7μF 20% 35V	26486-219P
C3	Tant 4.7μF 20% 35V	26486-219P
C4	Tant 4.7μF 20% 35V	26486-219P
C5	Cer 0.022μF -20+50% 18V	26383-007R
C6	Cer 0.022μF -20+50% 18V	26383-007R
C7 to C23	Cer 0.01μF -20+80% 100V	26383-055L
C24	Cer 0.001μF 10% 63V	26383-585M
C25	Cer 0.01μF -20+80% 100V	26383-055L
C26	Cer 0.001μF 10% 63V	26383-585M
C27 to C32	Cer 0.01μF -20+80% 100V	26383-055L
C33	Cer 0.001μF 10% 63V	26383-585M
C34 to C37	Cer 0.01μF -20+80% 100V	26383-055L
C38	Plas 0.01μF 1% 160V	26516-718Y
C39	Cer 0.047μF -20+80% 25V	26383-017U
C40	Cer 220pF 10% 63V	26383-595H
C41	Cer 220pF 10% 63V	26383-595H
C43	Tant 0.47μF 20% 35V	26486-207L
C44	Plas 0.001μF 2% 160V	26516-481L
C45	Cer 0.01μF -20+80% 100V	26383-055L
C46	Cer 22pF 5% 63V	26343-469N

17. Unit AL4 - Synchronizer/Counter 'B' (continued)

Circuit reference	Description	Code no.
C47	Plas 1.0µF 10% 63V	26582-414R
C48	Plas 0.0068µF 2% 160V	26516-924U
C49	Cer 0.01µF -20+80% 100V	26383-055L
C50	Tant 0.47µF 20% 35V	26486-207L
C51	Cer 22pF 5% 63V	26343-469N
C52	Cer 0.01µF -20+80% 100V	26383-055L
C53	Cer 0.01µF -20+80% 100V	26383-055L
C54	Tant 4.7µF 20% 35V	26486-219P
C55	Plas 0.22µF 10% 100V	26582-226G
C56	Cer 0.01µF -20+80% 100V	26383-055L
C57	Plas 0.1µF 10% 100V	26582-211B
C58	Cer 0.01µF -20+80% 100V	26383-055L
C59	Cer 0.01µF -20+80% 100V	26383-055L
C60	Elec 100µF -20+100% 25V	26415-813U
C61	Tant 22µF 20% 15V	26486-230B
C62	Plas 100pF ±2pF 350V	26516-243J
D1	Z5B20	28372-786A
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4148	28336-676J
D6	Z5B 8.2	28371-673Y
IC1	74LS390	28464-127R
IC2	74LS00	28466-345H
IC3	74LS00	28466-345H
IC4	74LS393	28464-130R
IC5	74LS390	28464-127R
IC6	74LS390	28464-127R
IC7	74LS51	28466-454N
IC8	74LS10	28466-351Y
IC9	74LS390	28464-127R
IC10	74LS90	28464-014S
IC11	74LS90	28464-014S
IC12	74LS00	28466-345H
IC13	74LS00	28466-345H
IC14	74LS02	28466-214Y
IC15	74LS27	28466-216L
IC16	74LS27	28466-216L
IC17	74LS390	28464-127R
IC18	74LS00	28466-345H
IC19	74LS20	28466-347U
IC20	74LS00	28466-345H
IC21	74LS00	28466-345H
IC22	74LS02	28466-214Y
IC23	74LS93	28464-117W
IC24	74LS00	28466-345H
IC25	74LS10	28466-351Y
IC26	74LS74	28462-611A

17. Unit AL4 - Synchronizer/Counter 'B' (continued)

Circuit reference	Description	Code no.
IC27	74LS27	28466-216L
IC28	74LS00	28466-345H
IC29	74LS74	28462-611A
IC30	74LS00	28466-345H
IC31	74LS74	28462-611A
IC32	74121	28468-402S
IC33	74121	28468-402S
IC34	74121	28468-402S
IC35	74LS74	28462-611A
IC36	74LS00	28466-345H
IC37	74LS90	28464-014S
R1	Met film 10kΩ 2% ¼W	24773-297M
R2	Met film 3.3kΩ 2% ¼W	24773-285F
R3	Met film 1kΩ 2% ¼W	24773-273A
R4	Met film 2.2kΩ 2% ¼W	24773-281Y
R6	Met film 470Ω 2% ¼W	24773-265M
R7	Met film 33kΩ 2% ¼W	24773-309Z
R10	Met film 15kΩ 2% ¼W	24773-301P
R11	Met film 10kΩ 2% ¼W	24773-297M
R12 †	Met film 330Ω 2% ¼W	24773-261D
R13	Var cermet 500Ω 10% ½W	25711-637F
R14	Met film 100kΩ 2% ¼W	24773-321L
R15	Met film 470Ω 2% ¼W	24773-265M
R16	Met film 22kΩ 2% ¼W	24773-305R
R17	Met film 10kΩ 2% ¼W	24773-297M
R18	Met film 1.5kΩ 2% ¼W	24773-277U
R19 †	Met film 1kΩ 2% ¼W	24773-273A
R20	Met film 47kΩ 2% ¼W	24773-313H
R21	Met film 1.5kΩ 2% ¼W	24773-277U
R22	Met film 22kΩ 2% ¼W	24773-305R
R23	Met film 22kΩ 2% ¼W	24773-305R
R24	Met film 22kΩ 2% ¼W	24773-305R
R25	Met film 270Ω 2% ¼W	24773-259T
R26	Met film 1kΩ 2% ¼W	24773-273A
R27	Met film 100kΩ 2% ¼W	24773-321L
R28	Met film 15kΩ 2% ¼W	24773-301P
R29	Met film 10kΩ 2% ¼W	24773-297M
R30	Met film 22Ω 2% ¼W	24773-233M
R31	Met film 10Ω 2% ¼W	24773-225W
R32	Met film 22Ω 2% ¼W	24773-233M
R33	Met film 22Ω 2% ¼W	24773-233M
TR1	BC237A	28455-421X
TR3	BC237A	28455-421X
TR4	2N4859A	28459-014T
TR5	J310	28459-028E
TR6	BC 237A	28455-421X

Circuit reference	Description	Code no.
	17. Unit AL4 - Synchronizer/Counter 'B' (continued)	
TR7	J310	28459-028E
TR8	E430	28459-031E
TR9	BC 237A	28455-421X
TR10	BC 308B	28433-455R
X1	10 MHz Crystal oscillator	44990-337E
	18. Unit AL5 - Synchronizer/Counter 'A'	
	Complete board	44828-328X
C1	Cer 0.01µF -20+100% 40V	26387-253M
C2	Cer 6.8pF ±0.5pF 63V	26343-463A
C3	Cer 0.01µF -20+80% 100V	26383-055L
C4	Cer 3.3pF ±0.5pF 63V	26343-459K
C5	Cer 3.3pF ±0.5pF 63V	26343-459K
C6	Cer 0.01µF -20+80% 100V	26383-055L
C7	Cer 0.001µF -20+80% 500V	26383-242P
C8	Cer 0.01µF -20+80% 100V	26383-055L
C9	Plas 0.1µF 10% 100V	26582-211B
C10	Cer 0.01µF -20+80% 100V	26383-055L
C11	Cer 0.01µF -20+80% 100V	26383-055L
C12	Cer 3.3pF ±0.5pF 63V	26343-459K
C13	Cer 0.01µF -20+80% 100V	26383-055L
C14	Cer 0.01µF -20+80% 100V	26383-055L
C15	Cer 0.047µF -20+80% 25V	26383-017U
C16	Cer 0.01µF -20+80% 100V	26383-055L
C17	Cer 2.7pF ±0.5pF 63V	26343-458B
C18	Cer 0.01µF -20+80% 100V	26383-055L
C19	Cer 0.01µF -20+80% 100V	26383-055L
C21	Cer 0.01µF -20+80% 100V	26383-055L
C22	Cer 0.001µF 10% 63V	26383-585M
C23	Cer 0.001µF 10% 63V	26383-585M
C24	Cer 0.001µF 10% 63V	26383-585M
C25	Cer 0.01µF -20+80% 100V	26383-055L
C26	Cer 0.001µF 10% 63V	26383-585M
C27	Cer 0.001µF 10% 63V	26383-585M
C28	Cer 0.01µF -20+80% 100V	26383-055L
C29	Cer 0.01µF -20+80% 100V	26383-055L
C30	Cer 0.01µF -20+80% 100V	26383-055L
C31	Cer 0.001µF 10% 63V	26383-585M
C32	Cer 0.01µF -20+80% 100V	26383-055L
C33	Elec 220µF -20+100% 10V	26415-817J
C34	Cer 0.01µF -20+80% 100V	26383-055L
C35	Cer 0.01µF -20+80% 100V	26383-055L
C36	Cer 0.01µF -20+80% 100V	26383-055L
C37	Cer 4.7pF ±0.5pF 63V	26343-461B
C38 to C42	Cer 0.01µF -20+80% 100V	26383-055L

18. Unit AL5 - Synchronizer/Counter 'A' (continued)

Circuit reference	Description	Code no.
C43	Cer 4.7pF ±0.5pF 63V	26343-461B
C44	Cer 0.01µF -20+80% 100V	26383-055L
C45	Cer 0.01µF -20+80% 100V	26383-055L
C47	Cer 0.01µF -20+80% 100V	26383-055L
C48	Cer 0.01µF -20+80% 100V	26383-055L
C49	Cer 0.047µF -20+80% 25V	26383-017U
C50 to C55	Cer 0.01µF -20+80% 100V	26383-055L
C56	Elec 47µF 20% 6V	26486-232A
C57 to C60	Cer 0.01µF -20+80% 100V	26383-055L
C61	Cer 0.01µF -20+100% 40V	26387-253M
C62 to C64	Cer 0.01µF -20+80% 100V	26383-055L
C65	Cer 0.001µF 10% 63V	26383-585M
C66	Elec 47µF 20% 6V	26486-232A
C67	Cer 0.01µF -20+80% 100V	26383-055L
C68	Cer 0.01µF -20+80% 100V	26383-055L
C69	Cer 0.01µF -20+80% 100V	26383-055L
C70	Cer 3.3pF ±0.5pF 63V	26343-459K
C71	Cer 3.3pF ±0.5pF 63V	26343-459K
C72	Cer 10pF ±0.5pF 63V	26343-465H
C73	Cer 180pF 10% 63V	26383-594Z
D1	1N5390	28349-005Z
D2	1N4148	28336-676J
D3 to D6	1N5390	28349-005Z
D7 to D11	1N4148	28336-676J
IC1	~~SP8646B~~ Superseded by SP8647B	28464-015W
IC2	74LS00	28466-345H
IC3	74S10	28466-338B
IC4	74LS04	28469-171L
IC5	SP8607B	28462-023B
IC6	SP8604B	28462-022R
IC7	74S00N	28466-331D
IC8	74LS00	28466-345H
IC9	74S00N	28466-331D
IC10	MC10106P	28466-222G
IC11	MC10102P	28466-219G
IC12	74H30	28466-330W
IC13	74S196	28464-010J
IC14	MC10125P	28469-380F

18. Unit AL5 - Synchronizer/Counter 'A' (continued)

Circuit reference	Description	Code no.
IC15	MC10138P	28464-019X
IC16	74LS00	28466-345H
IC17 to IC20	74LS251	28469-710B
IC21	74S196	28464-010J
IC22	74LS196	28464-016D
IC23	74LS196	28464-016D
IC24	74LS00	28466-345H
IC25	74LS30	28466-348Y
IC26	74LS02	28466-214Y
IC27	74LS93	28464-117W
IC28	74LS00	28466-345H
IC29	74LS02	28466-214Y
IC30 to IC33	74LS196	28464-016D
IC34 to IC37	74LS164	28467-515G
IC38	74LS51	28466-454N
RLA	80-1-A-5/620	23486-503E
RLB	80-1-A-5/620	23486-503E

Circuit reference	Description	Code no.
R1	Carb 43Ω 5% 1/8W	24331-995C
R2	Met film 430Ω 2% ¼W	24773-264X
R3	Met film 56Ω 2% ¼W	24773-243H
R4	Met film 270Ω 2% ¼W	24773-259T
R5	Met film 24kΩ 2% ¼W	24773-306B
R6	Met film 2kΩ 2% ¼W	24773-280U
R7	Carb 82Ω 5% 1/8W	24331-996R
R8	Met film 270Ω 2% ¼W	24773-259T
R9	Met film 24kΩ 2% ¼W	24773-306B
R10	Met film 2kΩ 2% ¼W	24773-280U
R11	Met film 680Ω 2% ¼W	24773-269K
R12	Met film 1.5kΩ 2% ¼W	24773-277U
R13	Met film 2kΩ 2% ¼W	24773-280U
R14	Carb 100Ω 5% 1/8W	24331-997B
R15	Met film 270Ω 2% ¼W	24773-259T
R16	Met film 24kΩ 2% ¼W	24773-306B
R17	Met film 2kΩ 2% ¼W	24773-280U
R18	Carb 82Ω 5% 1/8W	24331-996R
R19 †	Met film 1kΩ 2% ¼W	24773-273A
R20	Met film 10kΩ 2% ¼W	24773-297M
R21	Met film 330kΩ 2% ¼W	24773-333P
R22	Carb 100Ω 5% 1/8W	24331-997B
R23	Carb 6.8MΩ 10% 1/8W	24321-883V
R24	Carb 2.2MΩ 10% 1/8W	24321-877J
R25	Met film 150Ω 2% ¼W	24773-253F

18. Unit AL5 - Synchronizer/Counter 'A' (continued)

Circuit reference	Description	Code no.
R26	Met film 6.8kΩ 2% ¼W	24773-293D
R27	Met film 2.2kΩ 2% ¼W	24773-281Y
R28	Met film 15kΩ 2% ¼W	24773-301P
R29	Met film 300Ω 2% ¼W	24773-260W
R30	Met film 1kΩ 2% ¼W	24773-273A
R31	Met film 100Ω 2% ¼W	24773-249J
R32	Met film 2.2kΩ 2% ¼W	24773-281Y
R33	Met film 6.8kΩ 2% ¼W	24773-293D
R34	Met film 3kΩ 2% ¼W	24773-284J
R35	Met film 1.3kΩ 2% ¼W	24773-276E
R36	Met film 47Ω 2% ¼W	24773-241A
R37	Met film 1.5kΩ 2% ¼W	24773-277U
R38	Met film 3kΩ 2% ¼W	24773-284J
R39	Met film 1.3kΩ 2% ¼W	24773-276E
R40	Met film 4.3kΩ 2% ¼W	24773-288S
R41	Met film 3kΩ 2% ¼W	24773-284J
R42	Met film 1.3kΩ 2% ¼W	24773-276E
R43	Met film 4.3kΩ 2% ¼W	24773-288S
R44	Met film 470Ω 2% ¼W	24773-265M
R45	Met film 470Ω 2% ¼W	24773-265M
R46	Met film 2kΩ 2% ¼W	24773-280U
R47	Met film 2kΩ 2% ¼W	24773-280U
R48	Met film 3kΩ 2% ¼W	24773-284J
R49	Met film 3.9kΩ 2% ¼W	24773-287V
R50	Met film 1.3kΩ 2% ¼W	24773-276E
R51	Met film 1kΩ 2% ¼W	24773-273A
R52	Met film 1kΩ 2% ¼W	24773-273A
R53	Met film 1kΩ 2% ¼W	24773-273A
R54	Met film 3.9kΩ 2% ¼W	24773-287V
R55	Met film 1.3kΩ 2% ¼W	24773-276E
R56	Met film 3kΩ 2% ¼W	24773-284J
R57	Met film 1kΩ 2% ¼W	24773-273A
R58	Met film 220Ω 2% ¼W	24773-257W
R59	Met film 470Ω 2% ¼W	24773-265M
R60 to R64	Met film 2kΩ 2% ¼W	24773-280U
R65	Met film 470Ω 2% ¼W	24773-265M
SKAB	Con assy.	23444-334Y
SKAC	Con assy.	23444-334Y
SK	(Mini jump shorting socket)	23435-990X
TR1	BFY90	28452-157R
TR2	BFY90	28452-157R
TR3	BFY90	28452-157R
TR4	BC238B	28452-781A
TR5	BC238B	28452-781A
TR6	BC308B	28433-455R
TR7	BC238B	28452-781A
TR8	2N2369	28452-197H
TR9	2N2369	28452-197H
TR10	2N2369	28452-197H

Circuit reference	Description	Code no.
	19. Unit AG1 - GPIB drive	
	Complete board	44828-387S
C1 to C8	Cer 0.01μF -20+100% 40V	26387-253M
D1	1N4148	28336-676J
IC1	74S38	28466-355F
IC2	74LS132	28469-205N
IC3	MC3448AP	28469-190R
IC4	MC3448AP	28469-190R
IC5	74LS245	28469-188B
IC6	74S132	28469-208F
IC7	74S09	28466-017S
IC8	74S04	28469-177W
R1	Resistor network 9 x 3.3kΩ	24681-612T
R3	Met film 3.3kΩ 2% ¼W	24773-285F
R4		
R5	Met film 3.3kΩ 2% ¼W	24773-285F
R6 to R13	Met film 6.8kΩ 2% ¼W	24773-293D
SF	6 position	23467-310C
SKR	Receptacle (24-way)	23435-133X
TR1	BC239	28452-771P
TR2	BC239	28452-771P
TR3	BC239	28452-771P
	20. Unit AA0 - RF Section 'A'	
C1 Ø to C64 Ø	Cer 0.001μF -20+80% 300V	26373-733K
L1 to L24	Choke 100μH 10%	23642-561W
L25 to L32	Inductor 6μH	44290-619Y
L33 to L38	Choke 100μH 10%	23642-561W
L39 to L44	Inductor 6 μH	44290-619Y
PLBX	Con. assy (PLBX-SKCN)	43129-543J
PLBY	Con. assy (PLBY-SKCZ)	43129-544F

Circuit reference	Description	Code no.
	20. Unit AA0 - RF Section 'A' (continued)	
SKCA	Con. assy.	43129-521T
SKCE	Con. assy.	43129-520D
SKCF	Bulkhead receptacle	23444-382T
SKCH	Bulkhead receptacle	23444-382T
SKCL	Con. assy.	43129-637E
	21. Unit AA11 - Divider chain	
	Complete board	44828-332M
C1	Cer 0.01µF -20+80% 100V	26383-055L
C2	Cer 0.01µF -20+80% 100V	26383-055L
C3	Cer 0.01µF -20+80% 100V	26383-055L
C4	Cer 0.039µF 20% 100V	26386-493F
C5	Cer 0.01µF -20+80% 100V	26383-055L
C6	Cer 0.01µF -20+80% 100V	26383-055L
C7	Cer 0.01µF -20+80% 100V	26383-055L
C8	Cer 0.001µF 10% 63V	26383-585M
C9	Cer 0.01µF -20+80% 100V	26383-055L
C10	Cer 0.001µF 10% 63V	26383-585M
C11	Cer 0.001µF 10% 63V	26383-585M
C12	Cer 0.001µF 10% 63V	26383-585M
C13	Cer 0.01µF -20+80% 100V	26383-055L
C14	Cer 0.001µF 10% 63V	26383-585M
C15	Cer 0.01µF -20+80% 100V	26383-055L
C16	Cer 0.001µF 10% 63V	26383-585M
C17	Cer 0.001µF 10% 63V	26383-585M
C18	Cer 0.01µF -20+80% 100V	26383-055L
C19	Cer 0.01µF -20+80% 100V	26383-055L
C20	Cer 0.001µF 10% 63V	26383-585M
C21	Cer 0.001µF 10% 63V	26383-585M
C22 to C29	Cer 0.01µF -20+80% 100V	26383-055L
C30	Cer 0.1µF -25+50% 30V	26383-031S
C31	Cer 0.1µF -25+50% 30V	26383-031S
C32	Cer 0.01µF -20+80% 100V	26383-055L
C33	Cer 0.01µF -20+80% 100V	26383-055L
C34	Cer 0.1µF -25+50% 30V	26383-031S
C35	Cer 0.1µF -25+50% 30V	26383-031S
C36	Cer 0.01µF-20+80% 100V	26383-055L
C37	Cer 0.01µF -20+80% 100V	26383-055L
C38	Cer 0.01µF -20+80% 100V	26383-055L
C39	Cer 0.039µF 20% 100V	26386-493F
C40	Cer 0.01µF -20+80% 100V	26383-055L
C41	Cer 0.039µF 20% 100V	26386-493F
C42	Cer 0.039µF 20% 100V	26386-493F
C43	Cer 0.01µF -20+80% 100V	26383-055L
C44	Cer 0.01µF -20+80% 100V	26383-055L
C45	Cer 3.3pF ±0.5pF 63V	26343-459K

21. Unit AA11 - Divider chain (continued)

Circuit reference	Description	Code no.
C46 to C51	Cer 0.01µF -20+80% 100V	26383-055L
C52	Cer 0.039µF 20% 100V	26386-493F
C53	Cer 4.7pF ±0.5pF 63V	26343-461B
C54	Cer 6.8pF ±0.5pF 63V	26343-463A
C55	Cer 4.7pF ±0.5pF 63V	26343-461B
C56	Cer 8.2pF ±0.5pF 63V	26343-464Z
C57	Cer 330pF ±0.5pF 63V	26343-483D
C58	Cer 33pF ±0.5pF 63V	26343-471Y
D1	1N4148	28336-676J
D2	BA482	28335-675R
D3	BA482	28335-675R
D4	1N4148	28336-676J
D5	BA482	28335-675R
D6	1N4148	28336-676J
D7	BA482	28335-675R
D8	1N4148	28336-676J
D9	BA482	28335-675R
D10	1N4148	28336-676J
D11	BA482	28335-675R
D12	1N4148	28336-676J
D13	BA482	28335-675R
D14	1N4148	28336-676J
D15	BA482	28335-675R
D16	1N4148	28336-676J
D17	1N4148	28336-676J
D18	BA482	28335-675R
IC1	7442	28465-003D
IC2	7400	28466-321L
IC3	SP8607B	28462-023B
IC4	MC10105	28466-105Z
IC6	MC1660L	28466-109Y
IC7	MC1670L	28462-603M
IC8	MC10105	28466-105Z
IC9	MC10131L	28462-605R
IC10	MC10105	28466-105Z
IC11	MC10105	28466-105Z
IC12	MC10131L	28462-605R
IC13	MC10105	28466-105Z
IC14	MC10105	28466-105Z
L3	Inductor 6µH	44290-619Y
L4	Inductor 6µH	44290-619Y
L5	Inductor 6µH	44290-619Y
L7	Inductor 6µH	44290-619Y
L9	Inductor 6µH	44290-619Y
L10	Inductor 6µH	44290-619Y
L12	Inductor 6µH	44290-619Y

21. Unit AA11 - Divider chain (continued)

Circuit reference	Description	Code no.
R1	Carb 51Ω 5% 1/8W	24331-989P
R2	Met film 4.7kΩ 2% ¼W	24773-289W
R3	Met film 1kΩ 2% ¼W	24773-273A
R4	Carb 51Ω 5% 1/8W	24331-989P
R5	Met film 100Ω 2% ¼W	24773-249J
R6	Carb 200Ω 5% 1/8W	24331-999A
R7	Met film 1kΩ 2% ¼W	24773-273A
R8	Met film 2kΩ 2% ¼W	24773-280U
R9	Met film 1kΩ 2% ¼W	24773-273A
R10	Met film 270Ω 2% ¼W	24773-259T
R11	Carb 16Ω 5% 1/8W	24331-987D
R12	Carb 51Ω 5% 1/8W	24331-989P
R13	Met film 240Ω 2% ¼W	24773-258D
R14	Met film 10kΩ 2% ¼W	24773-297M
R15	Met film 4.3kΩ 2% ¼W	24773-288S
R16	Met film 1kΩ 2% ¼W	24773-273A
R17	Carb 100Ω 5% 1/8W	24331-997B
R18	Met film 10kΩ 2% ¼W	24773-297M
R19	Met film 1.5kΩ 2% ¼W	24773-277U
R20	Met film 1.5kΩ 2% ¼W	24773-277U
R21	Met film 620Ω 2% ¼W	24773-268B
R22	Met film 2.2kΩ 2% ¼W	24773-281Y
R23	Met film 3.9kΩ 2% ¼W	24773-287V
R24	Met film 2.7kΩ 2% ¼W	24773-283L
R25	Met film 6.8kΩ 2% ¼W	24773-293D
R26	Met film 270Ω 2% ¼W	24773-259T
R27 to R32	Met film 470Ω 2% ¼W	24773-265M
R33	Met film 4.3kΩ 2% ¼W	24773-288S
R34	Met film 1kΩ 2% ¼W	24773-273A
R35	Met film 620Ω 2% ¼W	24773-268B
R36	Met film 2.2kΩ 2% ¼W	24773-281Y
R37 to R42	Met film 470Ω 2% ¼W	24773-265M
R43	Met film 4.3kΩ 2% ¼W	24773-288S
R44	Met film 1kΩ 2% ¼W	24773-273A
R45	Met film 620Ω 2% ¼W	24773-268B
R46	Met film 2.2kΩ 2% ¼W	24773-281Y
R47 to R50	Met film 470Ω 2% ¼W	24773-265M
R51	Met film 1.5kΩ 2% ¼W	24773-277U
R52	Met film 820Ω 2% ¼W	24773-271B
R54	Met film 470Ω 2% ¼W	24773-265M
R55	Met film 470Ω 2% ¼W	24773-265M
R56	Met film 4.3kΩ 2% ¼W	24773-288S

21. Unit AA11 - Divider chain (continued)

Circuit reference	Description	Code no.
R57	Met film 1kΩ 2% ¼W	24773-273A
R58	Met film 620Ω 2% ¼W	24773-268B
R59	Met film 2.2kΩ 2% ¼W	24773-281Y
R60	Met film 470Ω 2% ¼W	24773-265M
R61	Met film 470Ω 2% ¼W	24773-265M
R62	Met film 470Ω 2% ¼W	24773-265M
R63	Met film 470Ω 2% ¼W	24773-265M
R66	Carb 51Ω 5% 1/8W	24331-989P
R67	Met film 470Ω 2% ¼W	24773-265M
R68	Met film 470Ω 2% ¼W	24773-265M
R69	Met film 4.3kΩ 2% ¼W	24773-288S
R70	Met film 1kΩ 2% ¼W	24773-273A
R71	Met film 620Ω 2% ¼W	24773-268B
R72	Met film 2.2kΩ 2% ¼W	24773-281Y
R73 to R76	Met film 470Ω 2% ¼W	24773-265M
R77	Carb 16Ω 5% 1/8W	24331-987D
R78	Carb 16Ω 5% 1/8W	24331-987D
R79	Carb 16Ω 5% 1/8W	24331-987D
R80	Met film 470Ω 2% ¼W	24773-265M
R81	Met film 470Ω 2% ¼W	24773-265M
R82	Met film 4.3kΩ 2% ¼W	24773-288S
R83	Met film 620Ω 2% ¼W	24773-268B
R84	Met film 2.2kΩ 2% ¼W	24773-281Y
R85	Met film 470Ω 2% ¼W	24773-265M
R86	Met film 470Ω 2% ¼W	24773-265M
R90	Met film 270Ω 2% ¼W	24773-259T
R91	Carb 51Ω 5% 1/8W	24331-989P
R92	Met film 1kΩ 2% ¼W	24773-273A
R93	Met film 4.7kΩ 2% ¼W	24773-289W
R94	Met film 100Ω 2% ¼W	24773-249J
R95	Carb 22Ω 5% 1/8W	24331-988T
R96	Carb 43Ω 5% 1/8W	24331-995C
R97	Met film 4.7kΩ 2% ¼W	24773-289W
R98	Met film 1kΩ 2% ¼W	24773-273A
R99	Carb 33Ω 5% 1/8W	24331-978J
R100	Met film 100Ω 2% ¼W	24773-249J
R101	Met film 680Ω 2% ¼W	24773-269K
R102	Met film 10kΩ 2% ¼W	24773-297M
R103	Met film 1kΩ 2% ¼W	24773-273A
R104	Carb 150Ω 5% 1/8W	24331-990D
R105	Met film 47Ω 2% ¼W	24773-241A
R106	Met film 100Ω 2% ¼W	24773-249J
R107	Carb 10Ω 5% 1/8W	24331-974U
R108	Carb 6.8Ω 5% 1/8W	24331-957P
R109	Met film 3.6kΩ 2% ¼W	24773-286G
R110	Met film 7.5kΩ 2% ¼W	24773-294T

Circuit reference	Description	Code no.
	21. Unit AA11 - Divider chain (continued)	
R111	Met film 1kΩ 2% ¼W	24773-273A
R112	Carb 150Ω 5% 1/8W	24331-990D
R113	Met film 150Ω 2% ¼W	24773-253F
R114	Carb 16Ω 5% 1/8W	24331-987D
R115	Carb 16Ω 5% 1/8W	24331-987D
R116	Carb 82Ω 5% 1/8W	24331-996R
SKBX	Con. coaxial 50Ω	23444-334Y
SKBY	Con. coaxial 50Ω	23444-334Y
T1 to T6	Transformers	43590-090M
TR1	2N5179	28451-697Y
TR2	BC308B	28433-455R
TR3	BFR90	28452-167U
TR4	BFR99	28433-336F
TR5	2N5179	28451-697Y
TR6	BC308B	28433-455R
TR7	BFR90	28452-167U
TR8	BC308B	28433-455R
TR9	BFR96	28452-171Y
TR10	BC239C	28452-771P
TR11	BC308B	28433-455R
TR12	BFR90	28452-167U
X1	Bead assy.	41372-006T
	22. Unit AA21 - Amplitude modulator	
	Complete board	44828-333C
C1	Cer 0.039µF 20% 100V	26386-493F
C2	Cer 0.039µF 20% 100V	26386-493F
C3	Cer 0.01µF -20+80% 100V	26383-055L
C4	Cer 0.01µF -20+80% 100V	26383-055L
C5	Plas 0.047µF 10% 250V	26582-206C
C6	Plas 0.047µF 10% 250V	26582-206C
C7	Tant 4.7µF 20% 35V	26486-219P
C8	Tant 4.7µF 20% 35V	26486-219P
C9	Plas 0.033µF 10% 250V	26582-205M
C10	Tant 4.7µF 20% 35V	26486-219P
C11	Cer 0.039µF 20% 100V	26386-493F
C12	Tant 0.47µF 20% 35V	26486-207L
C13	Cer 0.039µF 20% 100V	26386-493F
C15	Cer 0.039µF 20% 100V	26386-493F
C16	Cer 0.039µF 20% 100V	26386-493F
C17	Tant 0.47µF 20% 35V	26486-207L
C19	Cer 0.039µF 20% 100V	26386-493F
C20	Cer 0.039µF 20% 100V	26386-493F
C21	Tant 0.47µF 20% 35V	26486-207L

22. Unit AA21 - Amplitude modulator (continued)

Circuit reference	Description	Code no.
C22	Cer 0.039μF 20% 100V	26386-493F
C24	Cer 0.039μF 20% 100V	26386-493F
C25	Cer 0.039μF 20% 100V	26386-493F
C27	Tant 0.47μF 20% 35V	26486-207L
C28 to C32	Cer 0.039μF 20% 100V	26386-493F
C33	Tant 0.47μF 20% 35V	26486-207L
C35	Cer 0.039μF 20% 100V	26386-493F
C36	Cer 0.039μF 20% 100V	26386-493F
C37	Cer 0.039μF 20% 100V	26386-493F
C38	Cer 0.039μF 20% 100V	26386-493F
C39	Tant 0.47μF 20% 35V	26486-207L
C40	Cer 0.039μF 20% 100V	26386-493F
C42	Cer 0.039μF 20% 100V	26386-493F
C44	Cer 0.001μF 10% 63V	26383-585M
C45	Cer 0.0012μF 10% 63V	26383-592K
C46	Cer 0.01μF -20+80% 100V	26383-055L
C47	Cer 0.01μF -20+100% 40V	26387-253M
C48	Cer 5pF 10% 300V	26333-227H
C49	Cer 68pF 2% 63V	26343-475F
C50	Cer 5pF 10% 300V	26333-227H
C52 †	Cer 1pF ±0.5pF 63V	26343-502Z
C53 †	Cer 1pF ±0.5pF 63V	26343-502Z
C54	Cer 0.001μF 10% 63V	26383-585M
C55	Cer 33pF 5% 63V	26343-471Y
D1	5082-3379	28383-997T
D2	5082-3379	28383-997T
D3 to D7	1N4148	28336-676J
D8	Z5B13	28372-213U
D9	1N4148	28336-676J
D10	1N4148	28336-676J
D11	Part of matched set (D11, D13, R119)	44529-059V
D12	1N4148	28336-676J
D13	Part of matched set (D11, D13, R119)	44529-059V
D14	1N4148	28336-676J
D16	1N4148	28336-676J
D17	1N4148	28336-676J
IC1	SE5534AH	28461-346K
IC2	N5556	28461-311C
L1	Inductor 4.7μH 10%	23642-553J
L3	Inductor 12μH	44190-029X
L7	Inductor 12μH	44190-029X
L10	Inductor 12μH	44190-029X

Circuit reference	Description	Code no.
	22. Unit AA21 - Amplitude modulator (continued)	
L13	Inductor 6μH	44290-619Y
L14	Inductor 12μH	44190-029X
L15	Inductor 12μH	44190-029X
L18	Inductor 6μH	44290-619Y
L19	Inductor 12μH	44190-029X
L20	Inductor 12μH	44190-029X
L24	Inductor 2.4μH 10%	44290-790U
RLA	Reed RS-12V	23486-427A
RLB	712-12 Teledyne	23486-118A
R1	Met film 2.7kΩ 2% ¼W	24773-283L
R2	Met film 1kΩ 2% ¼W	24773-273A
R3	Met film 470Ω 2% ¼W	24773-265M
R4	Met film 47kΩ 2% ¼W	24773-313H
R5	Met film 18kΩ 2% ¼W	24773-303M
R6	Met film 51kΩ 2% ¼W	24773-314E
R7	Met film 100kΩ 2% ¼W	24773-321L
R8	Met film 2.7kΩ 2% ¼W	24773-283L
R9	Met film 10kΩ 2% ¼W	24773-297M
R10	Met film 10kΩ 2% ¼W	24773-297M
R11†	Met film 1.6kΩ 2% ¼W	24773-278Y
R12	Met film 1kΩ 2% ¼W	24773-273A
R13	Met film 100Ω 2% ¼W	24773-249J
R14	Met film 620Ω 2% ¼W	24773-268B
R15	Met film 100Ω 2% ¼W	24773-249J
R16	Met film 1.8kΩ 2% ¼W	24773-279N
R17	Met film 330kΩ 2% ¼W	24773-333P
R18	Met film 330kΩ 2% ¼W	24773-333P
R19	Met film 10kΩ 2% ¼W	24773-297M
R20	Met film 100kΩ 2% ¼W	24773-321L
R21	Met film 8.2kΩ 2% ¼W	24773-295P
R22	Met film 12kΩ 2% ¼W	24773-299R
R23	Met film 3kΩ 2% ¼W	24773-284J
R24	Met film 560Ω 2% ¼W	24773-267R
R25	Met film 1.5kΩ 2% ¼W	24773-277U
R26	Met film 82Ω 2% ¼W	24773-247N
R27	Met film 200Ω 2% ¼W	24773-256S
R28	Met film 10kΩ 2% ¼W	24773-297M
R29	Met film 2.2kΩ 2% ¼W	24773-281Y
R30	Met film 10kΩ 2% ¼W	24773-297M
R31	Met film 2.2kΩ 2% ¼W	24773-281Y
R32	Met film 10kΩ 2% ¼W	24773-297M
R33	Met film 4.7kΩ 2% ¼W	24773-289W
R34	Met film 10kΩ 2% ¼W	24773-297M
R35	Met film 100kΩ 2% ¼W	24773-321L
R36	Met film 12kΩ 2% ¼W	24773-299R
R37†	Met film 82Ω 2% ¼W	24773-247N
R38	Met film 1.5kΩ 2% ¼W	24773-277U
R39	Met film 15kΩ 2% ¼W	24773-301P

22. Unit AA21 - Amplitude modulator (continued)

Circuit reference	Description	Code no.
R40	Met film 51Ω 2% ¼W	24773-242Z
R41	Met film 1kΩ 2% ¼W	24773-273A
R42	Met film 100Ω 2% ¼W	24773-249J
R43	Carb 200Ω 5% 1/8W	24331-999A
R44	Carb 16Ω 5% 1/8W	24331-987D
R45	Chip 16Ω 5%	24681-043E
R46	Met film 300Ω 2% ¼W	24773-260W
R47	Met film 8.2kΩ 2% ¼W	24773-295P
R48	Met film 1kΩ 2% ¼W	24773-273A
R49	Met film 150Ω 2% ¼W	24773-253F
R50	Met film 68Ω 2% ¼W	24773-245U
R51	Met film 10kΩ 2% ¼W	24773-297M
R52	Met film 1.5kΩ 2% ¼W	24773-277U
R53	Met film 10kΩ 2% ¼W	24773-297M
R54	Met film 51Ω 2% ¼W	24773-242Z
R55	Met film 1kΩ 2% ¼W	24773-273A
R56	Met film 100Ω 2% ¼W	24773-249J
R57	Carb 150Ω 5% 1/8W	24331-990D
R58	Carb 16Ω 5% 1/8W	24331-987D
R59	Chip 16Ω 5%	24681-043E
R60	Met film 22kΩ 2% ¼W	24773-305R
R61	Met film 3.6kΩ 2% ¼W	24773-286G
R62	Var cermet 1kΩ 10% ½W	25711-638G
R63	Met film 620Ω 2% ¼W	24773-268B
R64	Met film 10kΩ 2% ¼W	24773-297M
R65	Met film 10kΩ 2% ¼W	24773-297M
R66	Met film 10kΩ 2% ¼W	24773-297M
R67	Met film 3kΩ 2% ¼W	24773-284J
R68	Met film 1.5kΩ 2% ¼W	24773-277U
R69	Met film 51Ω 2% ¼W	24773-242Z
R70	Met film 9.1kΩ 2% ¼W	24773-296X
R71	Met film 1kΩ 2% ¼W	24773-273A
R72	Met film 180Ω 2% ¼W	24773-255V
R73	Carb 150Ω 5% 1/8W	24331-990D
R74	Carb 16Ω 5% 1/8W	24331-987D
R75	Chip 16Ω 5%	24681-043E
R76	Met film 4.7kΩ 2% ¼W	24773-289W
R77	Met film 51Ω 2% ¼W	24773-242Z
R78	Met film 13kΩ 2% ¼W	24773-300T
R79	Met film 1kΩ 2% ¼W	24773-273A
R80	Met film 51Ω 2% ¼W	24773-242Z
R81	Carb 150Ω 5% 1/8W	24331-990D
R82	Carb 16Ω 5% 1/8W	24331-987D
R84	Met film 330kΩ 2% ¼W	24773-333P
R85	Met film 100kΩ 2% ¼W	24773-321L
R86	Var cermet 100kΩ 10% ½W	25711-644W
R87	Met film 20Ω 2% ¼W	24773-232X
R88	Met film 22kΩ 2% ¼W	24773-305R

22. Unit AA21 - Amplitude modulator (continued)

Circuit reference	Description	Code no.
R89	Met film 4.7kΩ 2% ¼W	24773-289W
R90	Met film 51Ω 2% ¼W	24773-242Z
R91	Met film 15kΩ 2% ¼W	24773-301P
R92	Met film 1kΩ 2% ¼W	24773-273A
R93	Var cermet 100Ω 10% ½W	25711-635L
R94	Carb 150Ω 5% 1/8W	24331-990D
R95	Carb 16Ω 5% 1/8W	24331-987D
R96	Chip 16Ω 5%	24681-043E
R97	Met film 4.7kΩ 2% ¼W	24773-289W
R98	Met film 51Ω 2% ¼W	24773-242Z
R99	Met film 15kΩ 2% ¼W	24773-301P
R100	Met film 51Ω 2% ¼W	24773-242Z
R101	Met film 1kΩ 2% ¼W	24773-273A
R102	Carb 150Ω 5% 1/8W	24331-990D
R103	Carb 16Ω 5% 1/8W	24331-987D
R104	Chip 16Ω 5%	24681-043E
R105	Carb 39Ω 5% 1/8W	24331-994M
R106	Carb 150Ω 5% 1/8W	24331-990D
R107	Carb 150Ω 5% 1/8W	24331-990D
R108	Met film 10kΩ 2% ¼W	24773-297M
R109	Met film 3.3Ω 2% ¼W	24773-213U
R110	Met film 1.1kΩ 2% ¼W	24773-273A
R111	Met film 10kΩ 2% ¼W	24773-297M
R112	Met film 47kΩ 2% ¼W	24773-313H
R113	Carb 10Ω 5% 1/8W	24331-974U
R114	Carb 270Ω 5% 1/8W	24331-992P
R115	Met film 820Ω 2% ¼W	24773-271B
R116	Carb 4.3kΩ 5% 1/8W	24331-956T
R117	Carb 270Ω 5% 1/8W	24331-992P
R118	Carb 180Ω 5% 1/8W	24331-961X
R119	Part of matched set (D11, D13, R119)	44529-059V
R120	Met film 9.1kΩ 2% ¼W	24773-296X
R121	Var cermet 2kΩ 10% ½W	25711-639V
R122	Met film 6.8kΩ 2% ¼W	24773-293D
R123	Met film 6.2kΩ 2% ¼W	24773-292W
R124	Met film 5.1kΩ 2% ¼W	24773-290V
R125	Met film 2.7kΩ 2% ¼W	24773-283L
R126	Met film 1.5kΩ 2% ¼W	24773-277U
R127	Met film 1kΩ 2% ¼W	24773-273A
SKCB	Receptacle	23444-334Y
SKCC	Receptacle	23444-334Y
SKCJ	Receptacle	23444-334Y
SK	(Mini jump shorting socket)	23435-990X
TR1	BC237	28455-421X
TR2	J309	28459-029U
TR3	BC251	28435-227H
TR4	BC237	28455-421X

Circuit reference	Description	Code no.
	22. Unit AA21 - Amplitude modulator (continued)	
TR5	BC251	28435-227H
TR6	J310	28459-028E
TR7	BC251	28435-227H
TR8	B238	28452-781A
TR9	B238	28452-781A
TR10	BC252	28433-455R
TR11	BC252	28433-455R
TR12	BC252	28433-455R
TR13	BC252	28433-455R
TR14	J310	28459-028E
TR15	BCY71	28435-235L
TR16	BFR90	28452-167U
TR17	MAT01GH	28461-913F
TR18	BFR99	28433-336F
TR19	BC239C	28452-771P
TR20	BCY71	28435-235L
TR21	BFR96	28452-171Y
TR22	B238	28452-781A
TR23	BC239C	28452-771P
TR24	BCY71	28435-235L
TR25	BFR96	28452-171Y
TR26	BCY71	28435-235L
TR27	BFR96	28452-171Y
TR28	BC252	28433-455R
TR29	BC252	28433-455R
TR30	BCY71	28435-235L
TR31	BFR96	28452-171Y
TR32	BCY71	28435-235L
TR33	BFR96	28452-171Y
TR34	BC252	28433-455R
TR35	BCY71	28435-235L
TR37	E430	28459-031E
X1	Double balanced mixer TFM-2	28531-003Z
X2	Double balanced mixer TFM-2	28531-003Z
	23. Unit AA22 - RF sub-unit 'A'	
C1 Ø	Cer 0.001µF -20+80% 300V	26373-733K
C2 Ø	Cer 0.001µF -20+80% 300V	26373-733K
C3 Ø	Cer 0.001µF -20+80% 300V	26373-733K
C4 Ø	Cer 50pF 10% 300V	26333-229U
C5 Ø to C12Ø	Cer 0.001µF -20+80% 300V	26373-733K
C13Ø	Cer 50pF 10% 300V	26333-229U
C14Ø	Cer 0.001µF -20+80% 300V	26373-733K
C15Ø	Cer 0.001µF -20+80% 300V	26373-733K
C16Ø	Cer 0.001µF -20+80% 300V	26373-733K
C17Ø	Cer 2.2pF ±0.5pF 63V	26343-457R

Circuit reference	Description	Code no.
	23. Unit AA22 - RF sub-unit 'A' (continued)	
C18	Cer 0.001μF 10% 63V	26383-585M
C19	Cer 0.001μF 10% 63V	26383-585M
C20	Cer 0.001μF 10% 63V	26383-585M
C21 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C22 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C23	Cer 0.001μF 10% 63V	26383-585M
C24 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C25 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C26	Cer 0.001μF 10% 63V	26383-585M
C27 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C28 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C29	Cer 0.001μF 10% 63V	26383-585M
C30 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C31 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C32 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C33 Ø	Cer 500pF -20+80% 300V	26373-732B
C34 Ø	Plas 180pF 2% 350V	26516-306U
C35 Ø	Cer 500pF -20+80% 300V	26373-732B
C36 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C37	Plas 180pF 2% 350V	26516-306U
C38	Plas 180pF 2% 350V	26516-306U
C39 Ø	Cer 500pF -20+80% 300V	26373-732B
D1 to D5	5082-3379	28383-997T
D6	1N4148	28336-676J
D7	1N4148	28336-676J
D8	1N4148	28336-676J
L1	22μH 10%	23642-557S
L2	Inductor	44290-619Y
L3	330μH 10%	23642-564P
L4	330μH 10%	23642-564P
PLCB	Con. assy.	43129-536U
PLCC	Con. assy.	43129-537Y
R1	Carb 200Ω 5% 1/8W	24331-999A
R2	Met film 1kΩ 2% ¼W	24773-273A
R3	Met film 47Ω 2% ¼W	24773-241A
R4	Met film 820Ω 2% ¼W	24773-271B
R5	Met film 1kΩ 2% ¼W	24773-273A
R6	Carb 100Ω 5% 1/8W	24331-997B
R7	Met film 2.7kΩ 2% ¼W	24773-283L
R8	Met film 240Ω 2% ¼W	24773-258D
R9	Met film 200Ω 2% ¼W	24773-256S
R10	Carb 68Ω 5% 1/8W	24331-979F
R11	Carb 33Ω 5% 1/8W	24331-978J
R12	Met film 2.7kΩ 2% ¼W	24773-283L

Circuit reference	Description	Code no.
	23. Unit AA22 - RF sub-unit 'A' (continued)	
R13	Met film 240Ω 2% ¼W	24773-258D
R14	Met film 220Ω 2% ¼W	24773-257W
R15	Carb 33Ω 5% 1/8W	24331-978J
R16	Carb 33Ω 5% 1/8W	24331-978J
R17	Met film 2.7kΩ 2% ¼W	24773-283L
R18	Met film 300Ω 2% ¼W	24773-260W
R19	Met film 270Ω 2% ¼W	24773-259T
R20	Carb 51Ω 5% 1/8W	24331-989P
SKBZ	Bulkhead receptacle	23444-345W
SKCD	Con. assy.	43129-522P
TR1	BFR90	28452-167U
TR2	BFR90	28452-167U
TR3	BFR90	28452-167U
X1 to X8	Ferrite bead	41372-006T
	24. Unit AA23 - Pulse amplifier	
	Complete board	44828-334R
C1	Tant 4.7μF 20% 35V	26486-219P
C2	Tant 4.7μF 20% 35V	26486-219P
C3	Tant 4.7μF 20% 35V	26486-219P
R1	Met film 3kΩ 2% ¼W	24773-284J
R2	Met film 16kΩ 2% ¼W	24773-302X
R3	Var cermet 10kΩ 10% ½W	25711-641G
R4	Met film 3kΩ 2% ¼W	24773-284J
R5	Met film 10Ω 2% ¼W	24773-225W
R6	Met film 51Ω 2% ¼W	24773-242Z
R7	Met film 4.7kΩ 2% ¼W	24773-289W
R8	Met film 1.8kΩ 2% ¼W	24773-279N
TR1	BC108	28452-787N
TR2	PN4258	28431-767E
TR3	PN4258	28431-767E
	25. Unit AA24 - Pulse amplifier	
	Complete board	44828-335B
C1	Tant 4.7μF 20% 35V	26486-219P
C2	Cer 68pF 2% 63V	26343-475F
D1	1N4148	28336-676J
D2	1N4148	28336-676J
IC1	CA 3046	28461-901A
R1	Met ox 51Ω 2% ½W	24573-042D
R2	Met film 4.7kΩ 2% ¼W	24773-289W
R3	Met film 27kΩ 2% ¼W	24773-307K
R4	Met film 1kΩ 2% ¼W	24773-273A

Circuit reference	Description	Code no.
	25. Unit AA24 - Pulse amplifier (continued)	
R5	Met film 82Ω 2% ¼W	24773-247N
R6	Met film 30Ω 2% ¼W	24773-236B
R7	Met film 100Ω 2% ¼W	24773-249J
R8	Met film 200Ω 2% ¼W	24773-256S
	26. Unit AA25 - Phase detector	
	Complete board	44828-336K
C1	Cer 0.001μF 10% 63V	26383-585M
C2	Cer 0.001μF 10% 63V	26383-585M
C3	Tant 4.7μF 20% 35V	26486-219P
C4	Cer 0.039μF 20% 100V	26386-493F
C5	Cer 0.039μF 20% 100V	26386-493F
C6	Cer 0.039μF 20% 100V	26386-493F
C7	Cer 22pF 5% 63V	26343-469N
C8	Tant 0.47μF 20% 35V	26486-207L
C9	Tant 0.47μF 20% 35V	26486-207L
C10	Cer 6.8pF ±0.5pF 63V	26343-463A
C11	Cer 0.0047μF 2% 160V	26383-591B
C12	Cer 0.039μF 20% 100V	26386-493F
C13	Cer 100pF ±0.5pF 63V	26343-477V
C14	Cer 0.047μF -20+80% 12V	26383-016E
C15	Cer 47pF ±5% 63V	26343-473L
C16	Cer 47pF ±5% 63V	26343-473L
D2 to D5	Matched set of 4	44529-048E
IC1	SE 5534AH	28461-346K
R3	Met film 470Ω 2% ¼W	24773-265M
R4	Met film 1kΩ 2% ¼W	24773-273A
R5	Carb 10Ω 5% 1/8W	24331-974U
R6	Carb 150Ω 5% 1/8W	24331-990D
R7	Met film 33Ω 2% ¼W	24773-237K
R8	Met ox 120Ω 2% ½W	24573-051R
R9	Carb 51Ω 5% 1/8W	24331-989P
R10	Met film 470Ω 2% ¼W	24773-265M
R11	Met film 470Ω 2% ¼W	24773-265M
R12	Met film 510Ω 2% ¼W	24773-266C
R13	Met film 510Ω 2% ¼W	24773-266C
R14	Met film 30kΩ 2% ¼W	24773-308A
R15	Met film 2.2kΩ 2% ¼W	24773-281Y
R16	Met film 2.2kΩ 2% ¼W	24773-281Y
R17	Met film 1.2kΩ 2% ¼W	24773-275H
R18	Met film 10kΩ 2% ¼W	24773-297M
R19	Met film 22kΩ 2% ¼W	24773-305R
R20	Met film 10kΩ 2% ¼W	24773-297M
T1	Transformer	43590-092R

Circuit reference	Description	Code no.
	26. Unit AA25 - Phase detector (continued)	
TR1	2N5179	28451-697Y
TR2	BFR96	28452-171Y
TR3	2N4858	28459-037F
TR4	BC308B	28433-455R
	27. Unit AA26 - VCO's	
	Complete board	44828-372A
C1	Cer 0.039µF 20% 100V	26386-493F
C2	Cer 2.7pF ±0.5pF 63V	26343-458B
C3	Cer 0.039µF 20% 100V	26386-493F
C4	Cer 2.2pF ±0.5pF 63V	26343-457R
C5	Cer 2.2pF ±0.5pF 63V	26343-457R
C6	Cer 1.8pF ±0.5pF 63V	26343-456C
C7	Cer 0.039µF 20% 100V	26386-493F
C8	Cer 0.039µF 20% 100V	26386-493F
C9	Cer 5.6pF ±0.5pF 63V	26343-462K
C10	Cer 0.039µF 20% 100V	26386-493F
C11	Cer 0.01µF -20+80% 100V	26383-055L
C12	Cer 0.01µF -20+80% 100V	26383-055L
C13	Tant 22µF 20% 15V	26486-230B
D1	BB105	28381-096S
D2	BB105	28381-096S
D3	BB105	28381-096S
D4	BB105	28381-096S
D5	5082-3379	28383-997T
D6	BB105	28381-096S
D7	5082-3379	28383-997T
D8	LED (Red LLL7)	28624-105D
D9	LED (Red LLL7)	28624-105D
L1 to L4	Inductor 6µH	44290-619Y
L7 to L10	Inductor 6µH	44290-619Y
L12	Inductor 6µH	44290-619Y
R1	Met film 270Ω 2% ¼W	24773-259T
R2	Met film 470Ω 2% ¼W	24773-265M
R3	Met film 270Ω 2% ¼W	24773-259T
R4	Met film 470Ω 2% ¼W	24773-265M
R5	Met film 4.7kΩ 2% ¼W	24773-289W
R6	Met film 4.7kΩ 2% ¼W	24773-289W
R7	Met film 4.7kΩ 2% ¼W	24773-289W
R8	Met film 4.7kΩ 2% ¼W	24773-289W
R9	Met film 330Ω 2% ¼W	24773-261D
R10	Carb 10Ω 5% 1/8W	24331-974U
R11	Carb 43Ω 5% 1/8W	24331-995C

Circuit reference	Description	Code no.
	27. Unit AA26 - VCO's (continued)	
R12	Met film 270Ω 2% ¼W	24773-259T
R13	Carb 43Ω 5% 1/8W	24331-995C
R14	Met film 1kΩ 2% ¼W	24773-273A
R15	Carb 16Ω 5% 1/8W	24331-987D
R16	Carb 39Ω 5% 1/8W	24331-994M
R17	Carb 100Ω 5% 1/8W	24331-997B
R18	Carb 68Ω 5% 1/8W	24331-979F
R19	Carb 100Ω 5% 1/8W	24331-997B
R20	Met film 3.3kΩ 2% ¼W	24773-285F
R21	Met film 3.3kΩ 2% ¼W	24773-285F
R22	Met film 2.2Ω 2% ¼W	24773-209E
R23	Carb 150Ω 5% 1/8W	24331-990D
R24	Carb 150Ω 5% 1/8W	24331-990D
TR1	2N5109	28454-797G
TR2	2N5109	28454-797G
TR3	BFR90	28452-167U
TR4	BFR90	28452-167U
	28. Unit AA31 - LP filters	
	Complete board	44828-337A
C1	Cer 0.01μF -20+80% 100V	26383-055L
C2	Cer 0.01μF -20+80% 100V	26383-055L
C5	Tant 0.47μF 20% 35V	26486-207L
C6	Cer 0.039μF 20% 100V	26386-493F
C7	Tant 0.47μF 20% 35V	26486-207L
C8	Cer 0.039μF 20% 100V	26386-493F
C10	Cer 0.01μF -20+80% 100V	26383-055L
C11	Cer 0.039μF 20% 100V	26386-493F
C12	Tant 0.47μF 20% 35V	26486-207L
C13	Cer 0.039μF 20% 100V	26386-493F
C15	Cer 0.039μF 20% 100V	26386-493F
C16	Cer 0.01μF -20+100% 40V	26387-253M
C17	Plas 0.0012μF 2% 160V	26516-512E
C18	Plas 0.00169μF 2% 160V	26516-541A
C19	Plas 0.0012μF 2% 160V	26516-512E
C20	Cer 0.01μF -20+100% 40V	26387-253M
C21	Plas 820pF 2% 160V	26516-462X
C22	Plas 0.0012μF 2% 160V	26516-512E
C23	Plas 820pF 2% 160V	26516-462X
C24	Cer 0.01μF -20+100% 40V	26387-253M
C25	Plas 620pF 2% 160V	26516-434B
C26	Plas 820pF 2% 160V	26516-462X
C27	Plas 620pF 2% 160V	26516-434B
C28	Cer 0.01μF -20+100% 40V	26387-253M
C29	Plas 390pF 2% 350V	26516-389X
C30	Plas 560pF 2% 160V	26516-423W
C31	Plas 390pF 2% 350V	26516-389X
C32	Cer 0.01μF -20+100% 40V	26387-253M
C33	Cer 270pF 2% 63V	26343-482W

28. Unit AA31 - LP filters (continued)

Circuit reference	Description	Code no.
C34	Cer 27pF 5% 63V	26343-470U
C35	Cer 270pF 2% 63V	26343-482W
C36	Cer 150pF 2% 63V	26343-479W
C37	Cer 270pF 2% 63V	26343-482W
C38	Cer 27pF 5% 63V	26343-470U
C39	Cer 0.01µF -20+100% 40V	26387-253M
C40	Cer 220pF 2% 63V	26343-481S
C41	Cer 330pF 2% 63V	26343-483D
C42	Cer 220pF 2% 63V	26343-481S
C43	Cer 0.001µF 10% 63V	26383-585M
C44	Cer 150pF 2% 63V	26343-479W
C45	Cer 220pF 2% 63V	26343-481S
C46	Cer 150pF 2% 63V	26343-479W
C47	Cer 0.001µF 10% 63V	26383-585M
C48	Cer 100pF 2% 63V	26343-477U
C49	Cer 150pF 2% 63V	26343-479W
C50	Cer 100pF 2% 63V	26343-477U
C51	Cer 0.001µF 10% 63V	26383-585M
C52	Cer 68pF 2% 63V	26343-475F
C53	Cer 100pF 2% 63V	26343-477U
C54	Cer 27pF 5% 63V	26343-470U
C55	Cer 68pF 2% 63V	26343-475F
C56	Cer 0.001µF 10% 63V	26383-585M
C57	Cer 47pF 5% 63V	26343-473L
C58	Cer 68pF 2% 63V	26343-475F
C59	Cer 4.7pF ±0.5pF 63V	26343-461B
C60	Cer 47pF 5% 63V	26343-473L
C61	Cer 0.001µF 10% 63V	26383-585M
C62	Cer 33pF 5% 63V	26343-471Y
C63	Cer 68pF 2% 63V	26343-475F
C64	Cer 33pF 5% 63V	26343-471Y
C65	Cer 0.001µF 10% 63V	26383-585M
C66	Cer 22pF 5% 63V	26343-469N
C67	Cer 22pF 5% 63V	26343-469N
C68	Cer 22pF 5% 63V	26343-469N
C69	Cer 22pF 5% 63V	26343-469N
C70	Cer 0.001µF 10% 63V	26383-585M
C71	Cer 15pF 5% 63V	26343-467U
C72	Cer 22pF 5% 63V	26343-469N
C73	Cer 10pF ±0.5pF 63V	26343-465H
C74	Cer 15pF 5% 63V	26343-467U
C75	Cer 0.001µF 10% 63V	26383-585M
C76	Cer 4.7pF ±0.5pF 63V	26343-461B
C77	Cer 4.7pF ±0.5pF 63V	26343-461B
C78	Cer 10pF ±0.5pF 63V	26343-465H
C79	Cer 10pF ±0.5pF 63V	26343-465H
C80	Cer 4.7pF ±0.5pF 63V	26343-461B
C81	Cer 4.7pF ±0.5pF 63V	26343-461B
C82	Cer 0.001µF 10% 63V	26383-585M

28. Unit AA31 - LP filters (continued)

Circuit reference	Description	Code no.
C86	Cer 0.001µF 10% 63V	26383-585M
C90	Cer 0.01µF -20+80% 100V	26383-055L
C91	Cer 0.039µF 20% 100V	26386-493F
C92	Tant 0.47µF 20% 35V	26486-207L
C93	Cer 0.039µF 20% 100V	26386-493F
C95	Cer 0.039µF 20% 100V	26386-493F
C96	Cer 0.01µF -20+80% 100V	26383-055L
C97	Cer 1.8pF ±0.5pF 63V	26343-456C
C98	Cer 0.039µF 20% 100V	26386-493F
C99	Tant 0.47µF 20% 35V	26486-207L
C100	Cer 0.039µF 20% 100V	26386-493F
C102	Cer 0.039µF 20% 100V	26386-493F
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	Z5B 7.5	28371-603H
D4	5082-3379	28383-997T
D5	5082-3379	28383-997T
D6	Z5B 7.5	28371-603H
D7	5082-3379	28383-997T
D8	5082-3379	28383-997T
D9	Z5B 7.5	28371-603H
D10	5082-3379	28383-997T
D11	5082-3379	28383-997T
D12	Z5B 7.5	28371-603H
D13	5082-3379	28383-997T
D14	5082-3379	28383-997T
D15	Z5B 7.5	28371-603H
D16	5082-3379	28383-997T
D17	5082-3379	28383-997T
D18	Z5B 7.5	28371-603H
D19	5082-3379	28383-997T
D20	5082-3379	28383-997T
D21	Z5B 7.5	28371-603H
D22	5082-3379	28383-997T
D23	5082-3379	28383-997T
D24	Z5B 7.5	28371-603H
D25	5082-3379	28383-997T
D26	5082-3379	28383-997T
D27	Z5B 7.5	28371-603H
D28	5082-3379	28383-997T
D29	5082-3379	28383-997T
D30	Z5B 7.5	28371-603H
D31	5082-3379	28383-997T
D32	5082-3379	28383-997T
D33	Z5B 7.5	28371-603H
D34	5082-3379	28383-997T
D35	5082-3379	28383-997T
D36	Z5B 7.5	28371-603H

28. Unit AA31 - LP filters (continued)

Circuit reference	Description	Code no.
D37	5082-3379	28383-997T
D38	5082-3379	28383-997T
D39	Z5B 7.5	28371-603H
D40	5082-3379	28383-997T
D41	5082-3379	28383-997T
D42	Z5B 7.5	28371-603H
D43	5082-3379	28383-997T
D44	5082-3379	28383-997T
D45	Z5B 7.5	28371-603H
D46	5082-3379	28383-997T
D47	5082-3379	28383-997T
D48	Z5B 7.5	28371-603H
D49 to D54	5082-3379	28383-997T
D55	1N4148	28336-676J
D56	1N4148	28336-676J
IC1	74159	28465-032V
IC2	74LS26	28466-350U
IC3	74LS26	28466-350U
IC4	74LS26	28466-350U
L3	Inductor 6μH	44290-619Y
L6	Inductor 6μH	44290-619Y
L7	Inductor 1.5μH 5%	23642-494P
L8	Inductor 1.5μH 5%	23642-494P
L9	Inductor 1μH 5%	23642-464M
L10	Inductor 1μH 5%	23642-464M
L11	Inductor 0.75μH 5%	23642-463X
L12	Inductor 0.75μH 5%	23642-463X
L13	Inductor 0.51μH 5%	23642-462P
L14	Inductor 0.51μH 5%	23642-462P
L15	Inductor 0.36μH 5%	23642-461T
L16	Inductor 0.36μH 5%	23642-461T
L17	Inductor 0.24μH 5%	23642-460D
L18	Inductor 0.24μH 5%	23642-460D
L19	Inductor 0.192μH	44290-762J
L20	Inductor 0.192μH	44290-762J
L21	Inductor 0.133μH	44290-763F
L22	Inductor 0.133μH	44290-763F
L23	Inductor 0.096μH	44290-764G
L24	Inductor 0.096μH	44290-764G
L25	Inductor 0.066μH	44290-765V
L26	Inductor 0.066μH	44290-765V
L27	Inductor 0.048μH	44290-766S
L28	Inductor 0.048μH	44290-766S
L29	Inductor 0.033μH	44290-767W
L30	Inductor 0.033μH	44290-767W

Circuit reference	Description	Code no.
	28. Unit AA31 - LP filters (continued)	
L41	Inductor 6μH	44290-619Y
L45	Inductor 6μH	44290-619Y
R1	Met film 22kΩ 2% ¼W	24773-305R
R2	Met film 1kΩ 2% ¼W	24773-273A
R3	Met film 2.2Ω 2% ¼W	24773-209E
R4	Carb 150Ω 5% 1/8W	24331-990D
R5	Carb 39Ω 5% 1/8W	24331-994M
R6	Carb 150Ω 5% 1/8W	24331-990D
R7	Met film 4.7kΩ 2% ¼W	24773-289W
R8	Met film 12kΩ 2% ¼W	24773-299R
R9	Met film 1kΩ 2% ¼W	24773-273A
R10	Carb 150Ω 5% 1/8W	24331-990D
R11	Met film 51Ω 2% ¼W	24773-242Z
R12	Met film 27Ω 2% ¼W	24773-235R
R13	Carb 16Ω 5% 1/8W	24331-987D
R14	Chip 16Ω 5%	24681-043E
R15	Met film 4.7kΩ 2% ¼W	24773-289W
R16	Met film 12kΩ 2% ¼W	24773-299R
R17	Met film 470Ω 2% ¼W	24773-273A
R18	Carb 150Ω 5% 1/8W	24331-990D
R19	Met film 51Ω 2% ¼W	24773-242Z
R20	Met film 27Ω 2% ¼W	24773-235R
R21	Carb 16Ω 5% 1/8W	24331-987D
R22	Chip 16Ω 5%	24681-043E
R23	Met film 470Ω 2% ¼W	24773-265M
R24	Met film 2.2kΩ 2% ¼W	24773-281Y
R25	Met film 3.9kΩ 2% ¼W	24773-287V
R26	Met film 22kΩ 2% ¼W	24773-305R
R27	Met film 470Ω 2% ¼W	24773-265M
R28	Met film 2.2kΩ 2% ¼W	24773-281Y
R29	Met film 3.9kΩ 2% ¼W	24773-287V
R30	Met film 22kΩ 2% ¼W	24773-305R
R31	Met film 470Ω 2% ¼W	24773-265M
R32	Met film 2.2kΩ 2% ¼W	24773-281Y
R33	Met film 3.9kΩ 2% ¼W	24773-287V
R34	Met film 22kΩ 2% ¼W	24773-305R
R35	Met film 470Ω 2% ¼W	24773-265M
R36	Met film 2.2kΩ 2% ¼W	24773-281Y
R37	Met film 3.9kΩ 2% ¼W	24773-287V
R38	Met film 22kΩ 2% ¼W	24773-305R
R39	Met film 470Ω 2% ¼W	24773-265M
R40	Met film 2.2kΩ 2% ¼W	24773-281Y
R41	Met film 3.9kΩ 2% ¼W	24773-287V
R42	Met film 22kΩ 2% ¼W	24773-305R
R43	Met film 470Ω 2% ¼W	24773-265M
R44	Met film 2.2kΩ 2% ¼W	24773-281Y
R45	Met film 3.9kΩ 2% ¼W	24773-287V
R46	Met film 22kΩ 2% ¼W	24773-305R

28. Unit AA31 - LP filters (continued)

Circuit reference	Description	Code no.
R47	Met film 470Ω 2% ¼W	24773-265M
R48	Met film 2.2kΩ 2% ¼W	24773-281Y
R49	Met film 3.9kΩ 2% ¼W	24773-287V
R50	Met film 22kΩ 2% ¼W	24773-305R
R51	Met film 470Ω 2% ¼W	24773-265M
R52	Met film 2.2kΩ 2% ¼W	24773-281Y
R53	Met film 3.9kΩ 2% ¼W	24773-287V
R54	Met film 22kΩ 2% ¼W	24773-305R
R55	Met film 470Ω 2% ¼W	24773-265M
R56	Met film 2.2kΩ 2% ¼W	24773-281Y
R57	Met film 3.9kΩ 2% ¼W	24773-287V
R58	Met film 22kΩ 2% ¼W	24773-305R
R59	Met film 470Ω 2% ¼W	24773-265M
R60	Met film 2.2kΩ 2% ¼W	24773-281Y
R61	Met film 3.9kΩ 2% ¼W	24773-287V
R62	Met film 22kΩ 2% ¼W	24773-305R
R63	Met film 470Ω 2% ¼W	24773-265M
R64	Met film 2.2kΩ 2% ¼W	24773-281Y
R65	Met film 3.9kΩ 2% ¼W	24773-287V
R66	Met film 22kΩ 2% ¼W	24773-305R
R67	Met film 470Ω 2% ¼W	24773-265M
R68	Met film 2.2kΩ 2% ¼W	24773-281Y
R69	Met film 3.9kΩ 2% ¼W	24773-287V
R70	Met film 22kΩ 2% ¼W	24773-305R
R71	Met film 470Ω 2% ¼W	24773-265M
R72	Met film 2.2kΩ 2% ¼W	24773-281Y
R73	Met film 3.9kΩ 2% ¼W	24773-287V
R74	Met film 22kΩ 2% ¼W	24773-305R
R75	Met film 470Ω 2% ¼W	24773-265M
R76	Met film 2.2kΩ 2% ¼W	24773-281Y
R77	Met film 3.9kΩ 2% ¼W	24773-287V
R78	Met film 22kΩ 2% ¼W	24773-305R
R79	Met film 470Ω 2% ¼W	24773-265M
R80	Met film 2.2kΩ 2% ¼W	24773-281Y
R81	Met film 3.9kΩ 2% ¼W	24773-287V
R82	Met film 22kΩ 2% ¼W	24773-305R
R83	Met film 5.1kΩ 2% ¼W	24773-290V
R84	Met film 2.2kΩ 2% ¼W	24773-281Y
R85	Met film 3.9kΩ 2% ¼W	24773-287V
R86	Met film 22kΩ 2% ¼W	24773-305R
R87	Met film 5.1kΩ 2% ¼W	24773-290V
R88	Met film 470Ω 2% ¼W	24773-265M
R89	Met film 4.7kΩ 2% ¼W	24773-289W
R90	Met film 12kΩ 2% ¼W	24773-299R
R91	Met film 1kΩ 2% ¼W	24773-273A
R92	Carb 150Ω 5% 1/8W	24331-990D
R93	Met film 51Ω 2% ¼W	24773-242Z
R94	Met film 27Ω 2% ¼W	24773-235R

Circuit reference	Description	Code no.
	28. Unit AA31 - LP filters (continued)	
R95	Carb 16Ω 5% 1/8W	24331-987D
R96	Chip 16Ω 5%	24681-043E
R97 †	Carb 33Ω 5% 1/8W	24331-978J
R98 †	Carb 22Ω 5% 1/8W	24331-988T
R99	Met film 4.7kΩ 2% ¼W	24773-289W
R100	Met film 13kΩ 2% ¼W	24773-300T
R101	Met film 1kΩ 2% ¼W	24773-273A
R102	Carb 150Ω 5% 1/8W	24331-990D
R103	Met film 51Ω 2% ¼W	24773-242Z
R104	Met film 33Ω 2% ¼W	24773-237K
R105	Carb 16Ω 5% 1/8W	24331-987D
R106	Chip 16Ω 5%	24681-043E
TR1	BC239C	28452-771P
TR2	BCY71	28435-235L
TR3	BFR96	28452-171Y
TR4	BCY71	28435-235L
TR5	BFR96	28452-171Y
TR6 to TR21	BC308B	28433-455R
TR22	BCY71	28435-235L
TR23	BFR96	28452-171Y
TR24	BCY71	28435-235L
TR25	BFR96	28452-171Y
X1	Ferrite bead	41372-006T
X2	Ferrite bead	41372-006T
	29. Unit AB0 - RF Section 'B'	
C1 Ø to C45 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C46	Plas 470pF 2% 160V	26516-406H
C47 Ø to C53 Ø	Cer 0.001μF -20+80% 300V	26373-733K
L1 to L14	Choke 100μH 10%	23642-561W
L15	Inductor 6μH	44290-619Y
L16	Inductor 6μH	44290-619Y
L17 to L24	Choke 100μH 10%	23642-561W
L25 to L30	Inductor 6 μH	44290-619Y
PLCP	Con. assy. (PLCP-SKDF)	43129-542L

Circuit reference	Description	Code no.
	29. Unit AB0 - RF Section 'B' (continued)	
PLCR	Con. assy.	43129-549D
PLCY	Con. assy. (PLCY-SKCK)	43129-541N
SKCR	Jack to jack, bulkhead adapter, 50 Ω	23444-303N
SKDB	Con. assy.	43129-554P
SKDC	Con. assy.	43129-555X
SKDD	Bulkhead receptacle 50Ω	23444-382T
SKDF	Con. assy. (SKDF-PLCP)	43129-542L
SKCK	Con. assy. (SKCK-PLCY)	43129-541N
SKCW	Con. assy.	43129-539L
SKCX	Con. assy	43129-540Y
X1	Ferrite bead	41372-006T
X2	Ferrite bead	41372-006T
	30. Unit AB1 - Range 1 frequency converter	
	Complete board	44828-338Z
C1	Cer 0.01μF -20+100% 40V	26387-253M
C2	Cer 0.047μF -20+80% 25V	26383-017U
C3	Tant 4.7μF 20% 35V	26486-219P
C4	Cer 0.01μF -20+80% 100V	26383-055L
C5	Cer 0.001μF 10% 63V	26383-585M
C6	Cer 0.01μF -20+80% 100V	26383-055L
C7	Cer 0.001μF 10% 63V	26383-585M
C8	Cer 0.01μF -20+80% 100V	26383-055L
C9	Cer 0.001μF 10% 63V	26383-585M
C10	Cer 0.001μF 10% 63V	26383-585M
C11	Cer 100pF 2% 63V	26343-477V
C12	Cer 150pF 5% 100V	26343-552W
C13	Cer 0.01μF -20+80% 100V	26383-055L
C14	Cer 0.01μF -20+80% 100V	26383-055L
C15	Cer 0.001μF 10% 63V	26383-585M
C16	Cer 470pF 5% 100V	26343-554T
C18	Cer 0.01μF -20+100% 40V	26387-253M
C19	Tant 4.7μF 20% 35V	26486-219P
C20 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C21 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C22	Cer 0.001μF 10% 63V	26383-585M
C23	Cer 0.01μF -20+80% 100V	26383-055L
C24	Cer 82pF 5% 100V	26343-551S
C25	Cer 0.01μF -20+80% 100V	26383-055L
C26	Cer 0.01μF -20+80% 100V	26383-055L
C27	Cer 0.01μF -20+80% 100V	26383-055L
C28	Cer 0.001μF 10% 63V	26383-585M
C29	Cer 0.01μF -20+80% 100V	26383-055L
C30	Tant 4.7μF 20% 35V	26486-219P
C31	Cer 27pF 5% 63V	26343-470U
C32	Cer 150pF 2% 63V	26343-479W
C33	Plas 820pF 2% 160V	26516-462X
C34	Cer 680pF 5% 100V	26343-555P

30. Unit AB1 - Range 1 frequency converter (continued)

Circuit reference	Description	Code no.
C35	Tant 2.2µF 20% 35V	26486-214V
C36	Tant 4.7µF 20% 35V	26486-219P
C37	Tant 4.7µF 20% 35V	26486-219P
C38	Cer 47pF 5% 63V	26343-473L
C39	Cer 0.001µF 10% 63V	26383-585M
C40	Cer 680pF 5% 100V	26343-555P
C41	Cer 150pF 2% 63V	26343-479W
C42	Cer 0.01µF -20+100% 40V	26383-253M
C43	Cer 0.001µF 5% 100V	26343-556X
C44	Cer 0.047µF -20+80% 25V	26383-017U
C45	Cer 0.01µF -20+80% 100V	26383-055L
C46	Cer 0.01µF -20+80% 100V	26383-055L
C47	Cer 0.01µF -20+80% 100V	26383-055L
C48	Cer 0.01µF -20+100% 40V	26383-253M
C49	Cer 150pF 2% 63V	26343-479W
C55	Cer 0.047µF -20+80% 25V	26383-017U
C56	Cer 680pF 5% 100V	26343-555P
C57	Cer 27pF 5% 100V	26343-553D
C58	Cer 680pF 5% 100V	26343-555P
C59	Cer 150pF 5% 100V	26343-552W
C60	Cer 0.01µF -20+80% 100V	26383-055L
C61	Cer 8.2pF 5% 100V	26343-464Z
D1	5022-3080	28383-999X
D2	Hot carrier diode FH1100	28349-005Z
D3	Hot carrier diode FH1100	28349-005Z
D4	Variable capacitor MV109	28381-130J
D5	Variable capacitor MV109	28381-130J
D9	1N4148	28336-676J
D10	1N4148	28336-676J
IC1 ⚠	4069	28469-191B
IC2 ⚠	4013	28462-608A
IC3 ⚠	4046	28461-917W
IC4	µA741C	28461-304T
L2	Inductor 33µH 10%	23642-558W
L3	Inductor 4.7µH 10%	23642-553J
L4	Inductor 1µH 10%	23642-549L
L5	Inductor assy. variable	44290-758L
L6	Inductor 0.47µH 10%	23642-547Y
L7	Inductor 2.2µH 10%	23642-551N
L8	Inductor assy. variable	44290-759J
L9	Inductor 33µH 10%	23642-558W
L10	Inductor assy. variable	44290-759J
L11	Inductor 6µH	44290-619Y
L12	Inductor 33µH 10%	23642-558W
L13	Inductor 33µH 10%	23642-558W
L14	Inductor assy. variable	44290-760N
L15	Inductor 4.7µH 10%	23642-553J
L16	Inductor assy. variable	44290-761L

30. Unit AB1 - Range 1 frequency converter (continued)

Circuit reference	Description	Code no.
R1	Met film 1kΩ 2% ¼W	24773-273A
R2	Met film 200kΩ 2% ¼W	24773-328D
R3	Var. cermet 100Ω 10% ½W	25711-635L
R5	Met film 43Ω 2% ¼W	24773-240K
R6	Met film 6.8kΩ 2% ¼W	24773-293D
R7	Met film 4.7kΩ 2% ¼W	24773-289W
R8	Met film 510Ω 2% ¼W	24773-266C
R9	Met film 200Ω 2% ¼W	24773-256S
R10	Met film 22Ω 2% ¼W	24773-233M
R11	Met film 11kΩ 2% ¼W	24773-298C
R12	Met film 3.9kΩ 2% ¼W	24773-287V
R13	Met film 1.1kΩ 2% ¼W	24773-274Z
R14	Met film 680Ω 2% ¼W	24773-269K
R15	Met film 22Ω 2% ¼W	24773-233M
R16	Met film 5.6kΩ 2% ¼W	24773-291S
R17	Met film 1.8kΩ 2% ¼W	24773-279N
R18	Met film 620Ω 2% ¼W	24773-268B
R19	Met film 220Ω 2% ¼W	24773-257W
R20	Met film 11kΩ 2% ¼W	24773-298C
R21	Met film 2.2kΩ 2% ¼W	24773-281Y
R22	Met film 100Ω 2% ¼W	24773-249J
R23	Met film 100Ω 2% ¼W	24773-249J
R24	Met film 100kΩ 2% ¼W	24773-321L
R25	Met film 13kΩ 2% ¼W	24773-300T
R26	Met film 100kΩ 2% ¼W	24773-321L
R27	Met film 100Ω 2% ¼W	24773-249J
R28	Met film 1kΩ 2% ¼W	24773-273A
R29	Met film 4.7kΩ 2% ¼W	24773-289W
R30	Met film 2.2kΩ 2% ¼W	24773-281Y
R31	Met film 430Ω 2% ¼W	24773-264X
R32	Met film 47Ω 2% ¼W	24773-241A
R33	Met film 1.6kΩ 2% ¼W	24773-278Y
R34	Met film 43Ω 2% ¼W	24773-240K
R35	Met film 3.9kΩ 2% ¼W	24773-287V
R36	Met film 8.2kΩ 2% ¼W	24773-295P
R37	Met film 1kΩ 2% ¼W	24773-273A
R38	Met film 1.2kΩ 2% ¼W	24773-275H
R39	Met film 1.8kΩ 2% ¼W	24773-279N
R40	Met film 150Ω 2% ¼W	24773-253F
R41	Met film 20Ω 2% ¼W	24773-232X
R42	Met film 1.5kΩ 2% ¼W	24773-277U
R43	Met film 750Ω 2% ¼W	24773-270R
R44	Met film 75Ω 2% ¼W	24773-246Y
R45	Met film 150Ω 2% ¼W	24773-253F
R46	Met film 39Ω 2% ¼W	24773-239Z
R47	Met film 150Ω 2% ¼W	24773-253F
R49	Met film 470kΩ 2% ¼W	24773-337R
R50	Met film 470kΩ 2% ¼W	24773-337R
R51	Met film 10kΩ 2% ¼W	24773-297M

Circuit reference	Description	Code no.
	30. Unit AB1 - Range 1 frequency converter (continued)	
R52	Met film 10kΩ 2% ¼W	24773-297M
R53	Met film 10kΩ 2% ¼W	24773-297M
R54	Met film 150Ω 2% ¼W	24773-253F
R55	Met film 4.7Ω 2% ¼W	24773-217J
R56	Met film 13kΩ 2% ¼W	24773-300T
R57	Met film 11kΩ 2% ¼W	24773-298C
R58	Met film 4.7kΩ 2% ¼W	24773-289W
R59	Met film 360Ω 2% ¼W	24773-262T
R60	Met film 100Ω 2% ¼W	24773-249J
R61	Met film 11kΩ 2% ¼W	24773-298C
R62	Met film 2.2kΩ 2% ¼W	24773-281Y
R63	Met film 100Ω 2% ¼W	24773-249J
R64	Met film 100Ω 2% ¼W	24773-249J
R65	Met film 12kΩ 2% ¼W	24773-299R
R66	Met film 4.7Ω 2% ¼W	24773-217J
R67	Met film 51Ω 2% ¼W	24773-242Z
R68	Met film 2.2Ω 2% ¼W	24773-209E
R69	Met film 12kΩ 2% ¼W	24773-299R
R70	Met film 39kΩ 2% ¼W	24773-311A
R71	Met film 150Ω 2% ¼W	24773-253F
T1	Transformer	43590-089R
TR1	2N5109	28454-797G
TR2	2N2369	28452-197H
TR3	2N2369	28452-197H
TR4	2N2369	28452-197H
TR5 ⚠	Dual gate FET 40673	28459-032U
TR6	BFR99	28433-336F
TR7	BFR99	28433-336F
TR8	2N5179	28451-697Y
TR9	2N5109	28454-797G
TR12	BCY70	28434-857Z
TR13	2N2369	28452-197H
TR15	BC308B	28433-455R
X1	Mixer, double balanced	28531-002A
X2	Surface acoustic wave filter	28531-011N
X3	Mixer, double balanced	28531-002A
X1	Crystal 31.5 MHz	28312-071C
	31. Unit AB2 - Output amplifiers and ALC	
	Complete board	44828-339H
C1	Tant 4.7μF 20% 35V	26486-219P
C2	Cer 0.022μF -25+50% 18V	26383-007R
C3	Cer 0.047μF -20+80% 25V	26383-017U
C4	Tant 4.7μF 20% 35V	26486-219P
C5	Cer 0.022μF -25+50% 18V	26383-007R
C6	Cer 0.001μF 10% 63V	26383-585M

31. Unit AB2 - Output amplifiers and ALC (continued)

Circuit reference	Description	Code no.
C7	Tant 4.7µF 20% 35V	26486-219P
C8	Tant 0.47µF 20% 35V	26486-207L
C9	Tant 4.7µF 20% 35V	26486-219P
C10	Tant 4.7µF 20% 35V	26486-219P
C11	Tant 0.47µF 20% 35V	26486-207L
C12	Tant 0.47µF 20% 35V	26486-207L
C13	Tant 4.7µF 20% 35V	26486-219P
C14	Cer 33pF 5% 63V	26343-471Y
C15	Cer 22pF 5% 63V	26343-469N
C16	Tant 0.47µF 20% 35V	26486-207L
C17	Cer 33pF 5% 63V	26343-471Y
C18	Elec 100µF -20+100% 25V	26415-813U
C19	Tant 0.47µF 20% 35V	26486-207L
C20	Plas 820pF 2% 160V	26516-462X
C21	Tant 4.7µF 20% 35V	26486-219P
C22	Cer 0.039µF 20% 100V	26386-493F
C24 †	Cer 1pF ±0.5pF 63V	26343-502Z
C25	Tant 4.7µF 20% 35V	26486-219P
C27	Cer 0.039µF 20% 100V	26386-493F
C28	Tant 0.47µF 20% 35V	26486-207L
C29	Cer 0.039µF 20% 100V	26386-493F
C30	Cer 0.039µF 20% 100V	26386-493F
C31 †	Cer 1.8pF ±0.5pF 63V	26343-456C
C32	Cer 0.001µF 10% 63V	26383-585M
C33	Cer 0.039µF 20% 100V	26386-493F
C34	Cer 1.8pF ±0.5pF 63V	26343-456C
C35	Cer 0.039µF 20% 100V	26386-493F
C36 †	Cer 1pF ±0.5pF 63V	26343-502Z
C38	Tant 0.47µF 20% 35V	26486-207L
C39	Cer 0.039µF 20% 100V	26386-493F
C40	Tant 0.47µF 20% 35V	26486-207L
C41	Cer 0.039µF 20% 100V	26386-493F
C42	Cer 0.0012µF 10% 63V	26383-592K
C43	Cer 1.8pF ±0.5pF 63V	26343-456C
C44	Cer 10pF ±0.5pF 63V	26343-465H
C45 †	Cer 1.5pF ±0.5pF 63V	26343-501A
C48	Cer 0.039µF 20% 100V	26386-493F
C49 †	Cer 1pF ±0.5pF 63V	26343-502Z
C51	Tant 0.47µF 20% 35V	26486-207L
C52	Cer 0.039µF 20% 100V	26386-493F
C53	Cer 0.039µF 20% 100V	26386-493F
C54	Cer 4.7pF ±0.5pF 63V	26343-461B
C55	Tant 4.7µF 20% 35V	26486-219P
C56	Cer 0.039µF 20% 100V	26386-493F
C57	Tant 0.47µF 20% 35V	26486-207L
C58	Cer 0.039µF 20% 100V	26386-493F
C59	Tant 4.7µF 20% 35V	26486-219P
C60	Tant 4.7µF 20% 35V	26486-219P
C61	Cer 4.7pF ±0.5pF 63V	26343-461B

31. Unit AB2 - Output amplifiers and ALC (continued)

Circuit reference	Description	Code no.
C62	Tant 4.7µF 20% 35V	26486-219P
C63	Tant 4.7µF 20% 35V	26486-219P
C64	Cer 0.039µF 20% 100V	26386-493F
C65	Tant 4.7µF 20% 35V	26486-219P
C66	Cer 47pF 10% 500V	26343-771K
C67	Cer 220pF 10% 200V	26343-772A
C68	Cer 82pF 2% 63V	26343-476G
C69	Cer 82pF 2% 63V	26343-476G
C70	Plas 0.1µF 10% 100V	26582-211B
C71	Cer 0.001µF 10% 63V	26383-585M
C72	Cer 82pF 2% 63V	26343-476G
C73	Cer 82pF 2% 63V	26343-476G
C74	Cer 82pF 2% 63V	26343-476G
C75	Cer 150pF 2% 63V	26343-479W
C76	Tant 0.47µF 20% 35V	26486-207L
C78	Cer 0.039µF 20% 100V	26386-493F
C79	Cer 220pF 2% 63V	26343-481S
D1	1N4148	28336-676J
D2	HP5082-3379	28383-997T
D3 to D7	HP5082-3080	28383-999X
D8 to D14	1N4148	28336-676J
D15 D16	Matched pair	44529-057F
D17 to D21	1N4148	28336-676J
D22	Z5B 6.8	28371-553P
D23	1N4148	28336-676J
D24	1N4148	28336-676J
D25	1N4148	28336-676J
IC1	µA725 HM	28461-345B
IC2	µA741 HM	28461-327F
IC3 ⚠	4016	28469-364K
IC4	µA741	28461-327F
IC5	CA 3046	28461-901A
IC6 ⚠	CA 3130S	28461-323Y
IC7 ⚠	4016	28469-364K
IC8 ⚠	CA 3130S	28461-323Y
IC9 ⚠	CA 3130S	28461-323Y
IC10 ⚠	CD 4024 RCA	28464-129K
IC11 ⚠	CA 3130S	28461-323Y
IC12 ⚠	CA 3130S	28461-323Y

31. Unit AB2 - Output amplifiers and ALC (continued)

Circuit reference	Description	Code no.
L1	Inductor 4.7μH 10%	23642-553J
L2	Inductor 2.2μH 10%	23642-551N
L3	Inductor 12μH	44190-029X
L5	Inductor 6μH	44290-619Y
L6	Inductor 6μH	44290-619Y
L7	Inductor 120μH	23642-601T
L8	Inductor 6μH	44290-619Y
L9	Inductor 1.5μH 10%	23642-550Y
L10	Inductor 22μH 10%	23642-557S
L11	Inductor 6μH	44290-619Y
L12	Inductor 6μH	44290-619Y
L13	Inductor 6μH	44290-619Y
L15	Inductor 22μH 10%	23642-557S
RLA	712-12 Teledyne	23486-118A
R1	Met film 300kΩ 2% ¼W	24773-332T
R2	Met film 1kΩ 2% ¼W	24773-273A
R3	Met film 2kΩ 2% ¼W	24773-280U
R4	Met film 100kΩ 2% ¼W	24773-321L
R5	Met film 39Ω 2% ¼W	24773-239Z
R6	Met film 10Ω 2% ¼W	24773-225W
R7	Met film 47kΩ 2% ¼W	24773-313H
R8	Met film 100kΩ 2% ¼W	24773-321L
R9	Met film 100kΩ 2% ¼W	24773-321L
R10	Met film 51Ω 2% ¼W	24773-242Z
R11	Met film 16kΩ 2% ¼W	24773-302X
R12	Met film 33kΩ 2% ¼W	24773-309Z
R13	Met film 270Ω 2% ¼W	24773-259T
R14	Met film 2kΩ 2% ¼W	24773-280U
R15	Met film 560Ω 2% ¼W	24773-267R
R16	Met film 300Ω 2% ¼W	24773-260W
R17	Met film 47kΩ 2% ¼W	24773-313H
R18	Met film 56kΩ 2% ¼W	24773-315U
R19	Met film 270Ω 2% ¼W	24773-259T
R20	Met film 270Ω 2% ¼W	24773-259T
R21	Met film 1MΩ 2% ¼W	24773-346E
R22	Met film 18kΩ 2% ¼W	24773-303M
R23	Met film 24kΩ 2% ¼W	24773-306B
R24	Met film 390Ω 2% ¼W	24773-263P
R25	Met film 100Ω 2% ¼W	24773-249J
R26	Met film 1.5kΩ 2% ¼W	24773-277U
R27	Met film 510Ω 2% ¼W	24773-266C
R28	Met film 200Ω 2% ¼W	24773-256S
R29	Met film 4.7kΩ 2% ¼W	24773-289W
R30	Met film 33Ω 2% ¼W	24773-237K
R31 †	Met film 10kΩ 2% ¼W	24773-297M
R32 †	Met film 10kΩ 2% ¼W	24773-297M
R33	Met film 1kΩ 2% ¼W	24773-273A
R34	Met film 2.2Ω 2% ¼W	24773-209E

31. Unit AB2 - Output amplifiers and ALC (continued)

Circuit reference	Description	Code no.
R35	Met film 2.2Ω 2% ¼W	24773-209E
R36	Met film 470Ω 2% ¼W	24773-265M
R37	Met film 47Ω 2% ¼W	24773-241A
R38	Met film 15kΩ 2% ¼W	24773-301P
R39	Met film 18kΩ 2% ¼W	24773-303M
R40	Met film 130Ω 2% ¼W	24773-252J
R41	Met film 30kΩ 2% ¼W	24773-308A
R42	Met film 100kΩ 2% ¼W	24773-321L
R43	Met film 8.2kΩ 2% ¼W	24773-295P
R44 †	Met film 12kΩ 2% ¼W	24773-299R
R45	Carb 150Ω 5% 1/8W	24331-990D
R46	Carb 22Ω 5% 1/8W	24331-988T
R47	Chip 16Ω 5%	24681-043E
R48	Met film 10Ω 2% ¼W	24773-225W
R49	Met film 62Ω 2% ¼W	24773-244E
R50	Met film 10Ω 2% ¼W	24773-225W
R51	Met film 1.2kΩ 2% ¼W	24773-275H
R52	Met film 1.2kΩ 2% ¼W	24773-275H
R53	Met film 330Ω 2% ¼W	24773-261D
R54	Met film 22Ω 2% ¼W	24773-233M
R55	Met film 1kΩ 2% ¼W	24773-273A
R56	Var cermet 1kΩ 10% ½W	25711-638G
R57	Met film 5.1kΩ 2% ¼W	24773-290V
R58	Carb 68Ω 5% 1/8W	24331-979F
R59	Met film 2.2Ω 2% ¼W	24773-209E
R60	Carb 150Ω 5% 1/8W	24331-990D
R61	Met film 3.9kΩ 2% ¼W	24773-287V
R62	Met film 1.5kΩ 2% ¼W	24773-277U
R63	Met film 15kΩ 2% ¼W	24773-301P
R64	Carb 150Ω 5% 1/8W	24331-990D
R65	Carb 22Ω 5% 1/8W	24331-988T
R66	Met film 56Ω 2% ¼W	24773-243H
R67	Met film 10Ω 2% ¼W	24773-225W
R68	Chip 16Ω 5%	24681-043E
R70	Met film 1.2kΩ 2% ¼W	24773-275H
R72	Met film 4.7Ω 2% ¼W	24773-217J
R73 †	Carb 270Ω 5% 1/8W	24331-992P
R74 †	Carb 16Ω 5% 1/8W	24331-987D
R75 †	Carb 270Ω 5% 1/8W	24331-992P
R76	Met film 15Ω 2% ¼W	24773-229X
R77	Met film 39kΩ 2% ¼W	24773-311A
R78	Met film 39kΩ 2% ¼W	24773-311A
R79	Met film 4.7kΩ 2% ¼W	24773-289W
R81	Met film 1.5kΩ 2% ¼W	24773-277U
R82	Carb 150Ω 5% 1/8W	24331-990D
R83	Carb 22Ω 5% 1/8W	24331-988T
R84	Met film 39Ω 2% ¼W	24773-239Z
R85	Met film 39Ω 2% ¼W	24773-239Z

31. Unit AB2 - Output amplifiers and ALC (continued)

Circuit reference	Description	Code no.
R86	Chip 16Ω 5%	24681-043E
R87	Carb 33Ω 5% 1/8W	24331-978J
R88	Met film 820Ω 2% ¼W	24773-271B
R89	Carb 51Ω 5% 1/8W	24331-989P
R90	Met ox 20Ω 2% ½W	24573-032L
R92	Carb 4.7Ω 5% 1/8W	24331-985S
R93	Carb 4.7Ω 5% 1/8W	24331-985S
R94	Met film 1.2kΩ 2% ¼W	24773-275H
R95	Met film 3.6kΩ 2% ¼W	24773-286G
R96	Var cermet 10kΩ 10% ½W	25711-641G
R97	Carb 100Ω 5% 1/8W	24331-997B
R98	Met film 4.7kΩ 2% ¼W	24773-289W
R99	Met film 470Ω 2% ¼W	24773-265M
R100	Var cermet 2kΩ 10% ½W	25711-639V
R101	Carb 22Ω 5% 1/8W	24331-988T
R102	Met film 1kΩ 2% ¼W	24773-273A
R103	Met ox 10Ω 2% ½W	24573-025E
R104	Met film 4.3kΩ 2% ¼W	24773-288S
R105	Chip 16Ω 5%	24681-043E
R106	Chip 16Ω 5%	24681-043E
R107	Met film 3.3kΩ 2% ¼W	24773-285F
R108	Non-inductive Met film 50 Ω 1% ¼W	24762-558R
R109	Met film 2.2Ω 2% ¼W	24773-209E
R110	Met film 470Ω 2% ¼W	24773-265M
R111	Met film 47kΩ 2% ¼W	24773-313H
R112	Met film 470kΩ 2% ¼W	24773-337R
R113	Met film 1.3kΩ 2% ¼W	24773-276E
R114	Met film 680Ω 2% ¼W	24773-269K
R115	Met film 1.5kΩ 2% ¼W	24773-277U
R116	Met film 5.6kΩ 2% ¼W	24773-291S
R117	Met ox 680Ω 2% ½W	24573-069S
R118	Met film 2.2kΩ 2% ¼W	24773-281Y
R119	Met film 470kΩ 2% ¼W	24773-337R
R121	Met film 100kΩ 2% ¼W	24773-321L
R122	Met film 2.2kΩ 2% ¼W	24773-281Y
R123	Met film 4.7kΩ 2% ¼W	24773-289W
R124	Met film 4.7kΩ 2% ¼W	24773-289W
R125	Met film 1kΩ 2% ¼W	24773-273A
R126	Met film 47kΩ 2% ¼W	24773-313H
R127	Met film 1MΩ 2% ¼W	24773-346E
R128	Met film 15kΩ 2% ¼W	24773-301P
R129	Met film 3.3kΩ 2% ¼W	24773-285F
R130	Met film 10kΩ 2% ¼W	24773-297M
R131	Met film 120Ω 2% ¼W	24773-251L
R132	Met film 15kΩ 2% ¼W	24773-301P
R133	Met film 150Ω 2% ¼W	24773-253F
R134	Met film 390Ω 2% ¼W	24773-263P
R135	Met film 5.6kΩ 2% ¼W	24773-291S
R136	Met film 39kΩ 2% ¼W	24773-311A

31. Unit AB2 - Output amplifiers and ALC (continued)

Circuit reference	Description	Code no.
R137	Var cermet 10kΩ 10% ½W	25711-603L
R138	Met film 300kΩ 2% ¼W	24773-332T
R141	Met film 300kΩ 2% ¼W	24773-332T
R142	Met film 20kΩ 2% ¼W	24773-304C
R143	Met film 82kΩ 2% ¼W	24773-319J
R144	Met film 150kΩ 2% ¼W	24773-325V
R145	Met film 27kΩ 2% ¼W	24773-307K
R146	Met film 3.3kΩ 2% ¼W	24773-285F
R147	Met film 10kΩ 2% ¼W	24773-297M
R148	Met film 10kΩ 2% ¼W	24773-297M
R149	Met film 10kΩ 2% ¼W	24773-297M
R150	Met film 10kΩ 2% ¼W	24773-297M
R151	Var cermet 100kΩ 10% ½W	25711-644W
R152	Met film 130kΩ 2% ¼W	24773-324G
R153	Var cermet 10kΩ 10% ½W	25711-641G
R154	Met film 100kΩ 2% ¼W	24773-321L
R155	Met film 47kΩ 2% ¼W	24773-313H
R156	Met film 10kΩ 2% ¼W	24773-297M
R157	Met film 100kΩ 2% ¼W	24773-321L
R158	Met film 130kΩ 2% ¼W	24773-324G
R159	Var cermet 100kΩ 10% ½W	25711-644W
R160	Carb film 3.3MΩ 10% 1/8W	24321-879G
R161	Met film 220kΩ 2% ¼W	24773-329T
R162	Met film 220kΩ 2% ¼W	24773-329T
R163	Met film 47kΩ 2% ¼W	24773-313H
R164	Met film 56kΩ 2% ¼W	24773-315U
R165	Met film 47kΩ 2% ¼W	24773-313H
R166	Met film 56kΩ 2% ¼W	24773-315U
R167	Met film 56kΩ 2% ¼W	24773-315U
R168	Met film 180kΩ 2% ¼W	24773-327W
R169	Met film 100kΩ 2% ¼W	24773-321L
R170	Met film 10kΩ 2% ¼W	24773-297M
R171	Met film 27kΩ 2% ¼W	24773-307K
R172	Met film 4.7kΩ 2% ¼W	24773-289W
R173	Met film 150kΩ 2% ¼W	24773-325V
R174	Met film 10kΩ 2% ¼W	24773-297M
R175	Met film 470kΩ 2% ¼W	24773-337R
R176	Met film 47kΩ 2% ¼W	24773-313H
R177	Met film 470kΩ 2% ¼W	24773-337R
R178	Met film 470kΩ 2% ¼W	24773-337R
R179	Met film 47kΩ 2% ¼W	24773-313H
R180	Met film 10kΩ 2% ¼W	24773-297M
R181	Met film 1MΩ 2% ¼W	24773-346E
R182	Met film 1MΩ 2% ¼W	24773-346E
R183	Met film 1MΩ 2% ¼W	24773-346E
R184	Met film 560kΩ 2% ¼W	24773-340R
R185	Met film 120kΩ 2% ¼W	24773-323F
R186	Met film 33kΩ 2% ¼W	24773-309Z
R187	Met film 100kΩ 2% ¼W	24773-321L

31. Unit AB2 - Output amplifiers and ALC (continued)

Circuit reference	Description	Code no.
R188	Met film 100kΩ 2% ¼W	24773-321L
R189	Met film 82kΩ 2% ¼W	24773-319J
R190	Met film 68kΩ 2% ¼W	24773-317N
R191	Met film 2.2kΩ 2% ¼W	24773-281Y
R192	Met film 3.3kΩ 2% ¼W	24773-285F
R193	Met film 150kΩ 2% ¼W	24773-325V
R194	Met film 150kΩ 2% ¼W	24773-325V
R195	Met film 150kΩ 2% ¼W	24773-325V
R196	Met film 150kΩ 2% ¼W	24773-325V
R197	Met film 150kΩ 2% ¼W	24773-325V
R198	Met film 150kΩ 2% ¼W	24773-325V
R199	Met film 150kΩ 2% ¼W	24773-325V
R200	Met film 75kΩ 2% ¼W	24773-318L
R201	Met film 75kΩ 2% ¼W	24773-318L
R202	Met film 75kΩ 2% ¼W	24773-318L
R203	Met film 75kΩ 2% ¼W	24773-318L
R204	Met film 75kΩ 2% ¼W	24773-318L
R205	Met film 75kΩ 2% ¼W	24773-318L
R206	Met film 150kΩ 2% ¼W	24773-325V
R207	Met film 2kΩ 2% ¼W	24773-280U
R208	Met film 47kΩ 2% ¼W	24773-313H
R209	Met film 56kΩ 2% ¼W	24773-315U
R210	Met film 68kΩ 2% ¼W	24773-317N
R211	Met film 56kΩ 2% ¼W	24773-315U
R212	Met film 56kΩ 2% ¼W	24773-315U
R213	Var cermet 100kΩ 10% ½W	25711-644W
R214	Met film 33kΩ 2% ¼W	24773-309Z
R215	Met film 56kΩ 2% ¼W	24773-315U
R216	Met film 47kΩ 2% ¼W	24773-313H
R217	Met film 22kΩ 2% ¼W	24773-305R
R218	Met film 1kΩ 2% ¼W	24773-273A
R219	Met film 33Ω 2% ¼W	24773-237K
R220	Met film 12Ω 2% ¼W	24773-227T
R221	Carb 1kΩ 5% 1/8W	24331-967A
R222	Met film 10kΩ 2% ¼W	24773-297M
SKCP	Right angled PWB receptacle	23444-388B
SKCY	Right angled PWB receptacle	23444-388B
TR1	Dual FET J412	28459-033Y
TR2	BCY 71	28435-235L
TR3	BC239C	28452-771P
TR4	BC252B	28433-455R
TR5	BC239C	28452-771P
TR6	BC239C	28452-771P
TR7	BCY 71	28435-235L
TR8	2N2219	28453-847F
TR9	2N2219	28453-847F
TR10	BD 135	28455-438J

Circuit reference	Description	Code no.
	31. Unit AB2 - Output amplifiers and ALC (continued)	
TR11	BD 135	28455-438J
TR12	BD 136	28435-238G
TR13	BC 239C	28452-771P
TR14	BCY 71	28435-235L
TR15	BFR 96	28452-171Y
TR16	BCY 71	28435-235L
TR18	BFR 96	28452-171Y
TR19	BC 252B	28433-455R
TR21	BCY 71	28435-235L
TR22	BFR 96	28452-171Y
TR23 △	BFQ34	28452-247V
TR24	BCY 71	28435-235L
TR25	BCY 71	28435-235L
TR26 △	BLW 32	28453-843Y
TR27	BC 107	28455-437L
TR28	BC 239C	28452-771P
TR29	MJE 711	28435-870M
TR30	BC 239C	28452-771P
TR31	2N2905	28434-879X
TR32	BDX 37	28456-775D
TR33	BDX 37	28456-775D
TR34	BC 252B	28433-455R
TR37	BC 252B	28433-455R
TR38	BC 252B	28433-455R
TR39	BC 252B	28433-455R
TR40	BC 239C	28452-771P
TR41	BC 239C	28452-771P
TR42	BC 252B	28433-455R
TR43	BC 252B	28433-455R
TR44	BC 239C	28452-771P
TR45	BC 239C	28452-771P
TR46	BC 239C	28452-771P
TR47	BC 239C	28452-771P
TR48	BC 252B	28433-455R
TR49	BC 239C	28452-771P
TR50	BC 239C	28452-771P
	32. Unit AB3 - Connector board	
	Complete board	44828-378N
	33. Unit AS1 - Master oscillator	
	Complete assy.	44990-301K
	Capacitor board (AS1C)	31828-386L
	Filter box assy.	41690-269W
	Gear box assy. (AS1A, for details see Chap. 7 Fig. 23)	41319-022R
C1 Ø	Cer 0.001µF -20+80% 300V	26373-733K

Circuit reference	Description	Code no.
	33. Unit AS1 - Master oscillator (continued)	
C2 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C3 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C6 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C7 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C8 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C10	Nose cone	34900-553W
C11	Tuning cone (part of L8)	33990-805K
C12	Oscillator tube	33900-804B
C13 Ø	Cer 500pF 25% 500V	26373-609F
C14 Ø	Cer 56pF 20% 500V	26373-855W
C15 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C16 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C17 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C18 Ø to C22 Ø	Cer 10pF ±1pF 300V	26333-228E
D1	1N5145 variable capacitor	28381-526K
L1	Choke 2.2μH	23642-551N
L2	Choke 2.2μH	23642-551N
L3	Inductor 6μH	44290-619Y
L5	Choke 2.2μH	23642-551N
L6	Choke 2.2μH	23642-551N
L8	Tuning cone (part of C11)	33900-805K
L9	Inductance	35902-682E
L12	Choke	34900-664C
L13	Choke	34900-664C
L14	Choke 2.2μH	23642-551N
L15	Choke 2.2μH	23642-551N
L16	Inductor 6μH	44290-619Y
L17	Choke 2.2μH	23642-551N
L18	Choke 2.2μH	23642-551N
L19	Choke 2.2μH	23642-551N
L20	Choke 2.2μH	23642-551N
R2	Carb 22Ω 5% 1/8W	23331-988T
R3	Carb 22Ω 5% 1/8W	24331-988T
R4	Met film 22Ω 2% ¼W	24773-233M
SKCM	Right angled bulkhead jack	23444-369J
TR1	BFR 91	28451-696U
X2	Ferrite bead	41372-006T
	34. Unit AS1B - Connector board	
	Complete board	44828-361T
	35. Unit AS2 - Latches	
	Complete board	44828-343E
C1 to C5	Cer 0.01μF -20+100% 40V	26387-253M

Circuit reference	Description	Code no.
	35. Unit AS2 - Latches (continued)	
C7	Cer 0.01µF -20+100% 40V	26387-253M
C8	Cer 0.01µF -20+100% 40V	26387-253M
C9	Cer 0.01µF -20+100% 40V	26387-253M
C11 to C16	Cer 0.01µF -20+100% 40V	26387-253M
IC1 to IC4	74LS373	28462-410E
IC6	74LS377	28462-619J
IC7	74LS377	28462-619J
IC8	74LS377	28462-619J
IC9	74LS377	28462-619J
IC11	74LS377	28462-619J
IC12	74LS154	28465-031G
IC13	74LS377	28462-619J
IC14	74LS377	28462-619J
IC15	74LS377	28462-619J
R1	Met film 10kΩ 2% ¼W	24773-297M
R2	Met film 220Ω 2% ¼W	24773-257W
R3	Met film 220Ω 2% ¼W	24773-257W
R4 R5 R8	Resistor network 47kΩ	24681-613P
SKBB		23435-145E
SKBC		23435-145E
SKBD		23435-145E
TR1	BC 238B	28452-781A
	36. Unit AS3 - Modulation leveller	
	Complete board	44828-344U
C1	Cer 0.01µF -20+100% 40V	26387-253M
C2	Cer 0.01µF -20+100% 40V	26387-253M
C3	Cer 22pF 5% 63V	26343-469N
C4	Cer 0.01µF -20+100% 40V	26387-253M
C5	Cer 0.01µF -20+100% 40V	26387-253M
C7	Elec 22µF -20+100% 25V	26415-805K
C9	Tant 22µF 20% 15V	26486-230B
C11	Tant 10µF 20% 35V	26486-225C
C12	Cer 0.01µF -20+100% 40V	26387-253M
C13	Cer 0.01µF -20+100% 40V	26387-253M
C15	Cer 0.01µF -20+100% 40V	26387-253M
C16	Cer 0.01µF -20+100% 40V	26387-253M
C17	Cer 22pF 5% 63V	26343-469N
C18	Cer 0.01µF -20+100% 40V	26387-253M
C19	Tant 4.7µF 20% 35V	26486-219P
C21	Plas 0.15µF 2% 63V	26582-405D
C22	Tant 4.7µF 20% 35V	26486-219P
C23	Cer 0.01µF -20+100% 40V	26387-253M

36. Unit AS3 - Modulation leveller (continued)

Circuit reference	Description	Code no.
C24	Cer 0.01μF -20+100% 40V	26387-253M
C25	Cer 150pF 2% 63V	26343-479W
C26	Plas 0.33μF 10% 63V	26582-408X
D1 to D8	1N4148	28336-676J
D9	Z5B 5.1	28371-403N
D10	1N4148	28336-676J
D11	1N4148	28336-676J
D12	1N4148	28336-676J
D13	Z5B 4.7	28371-373V
IC1	NE5534AH	28461-329V
IC2	NE538	28461-344R
IC3	N5556V	28461-311C
IC4	μA741C	28461-304T
IC6	NE5534AH	28461-329V
IC7	NE535	28461-343C
IC8	μA741C	28461-304T
IC9	DAC-08CQ	28469-395B
IC10	μA741C	28461-304T
R1	Var cermet 5kΩ 10% ½W	25711-610V
R2	Var cermet 5kΩ 10% ½W	25711-610V
R3	Var cermet 100kΩ 10% ½W	25711-613D
R4	Var cermet 10kΩ 10% ½W	25711-603L
R5	Var cermet 1kΩ 10% ½W	25711-602N
R6	Var cermet 100kΩ 10% ½W	25711-613D
R7	Var cermet 20kΩ 10% ½W	25711-611S
R8	Var cermet 5kΩ 10% ½W	25711-610V
R9	Var cermet 100Ω 10% ½W	25711-608S
R10	Var cermet 2kΩ 10% ½W	25711-609W
R12	Met film 10kΩ 2% ¼W	24773-297M
R13	Met film 5.1kΩ 2% ¼W	24773-290V
R14	Met film 22kΩ 2% ¼W	24773-305R
R15	Met film 2.0kΩ 2% ¼W	24773-280U
R16	Met film 9.1kΩ 2% ¼W	24773-296X
R17	Met film 9.1kΩ 2% ¼W	24773-296X
R18	Met film 10kΩ 2% ¼W	24773-297M
R19	Met film 360kΩ 2% ¼W	24773-334X
R20	Met film 36kΩ 2% ¼W	24773-310K
R21	Brimister	25683-644G
R22	Met film 27kΩ 2% ¼W	24773-307K
R23	Met film 22kΩ 2% ¼W	24773-305R
R24	Met film 15kΩ 2% ¼W	24773-301P
R25	Met film 270kΩ 2% ¼W	24773-331D
R26	Met film 4.3kΩ 2% ¼W	24773-288S
R27	Met film 5.1kΩ 2% ¼W	24773-290V
R28	Met film 2.0kΩ 2% ¼W	24773-280U

Circuit reference	Description	Code no.
	36. Unit AS3 - Modulation leveller (continued)	
R29	Met film 12kΩ 2% ¼W	24773-299R
R30	Met film 200kΩ 2% ¼W	24773-328D
R31	Met film 10kΩ 2% ¼W	24773-297M
R32	Met film 200kΩ 2% ¼W	24773-328D
R33	Met film 3kΩ 2% ¼W	24773-284J
R34	Met film 10kΩ 2% ¼W	24773-297M
R35	Met film 3.3kΩ 2% ¼W	24773-285F
R36	Met film 820Ω 2% ¼W	24773-271B
R37	Met film 2.2kΩ 2% ¼W	24773-281Y
R38	Met film 3.6kΩ 2% ¼W	24773-286G
R39	Met film 10kΩ 2% ¼W	24773-297M
R40	Met film 10kΩ 2% ¼W	24773-297M
R41	Met film 3.3kΩ 2% ¼W	24773-285F
R42	Met film 20kΩ 2% ¼W	24773-304C
R43	Met film 3.6kΩ 2% ¼W	24773-286G
R44	Met film 39kΩ 2% ¼W	24773-311A
R45	Met film 10kΩ 2% ¼W	24773-297M
R46	Met film 10kΩ 2% ¼W	24773-297M
R47	Met film 10kΩ 2% ¼W	24773-297M
R48	Met film 5.6kΩ 2% ¼W	24773-291S
R49	Met film 10kΩ 2% ¼W	24773-297M
R50	Met film 10kΩ 2% ¼W	24773-297M
R51	Met film 10kΩ 2% ¼W	24773-297M
R52	Met film 10kΩ 2% ¼W	24773-297M
R53	Met film 5.6kΩ 2% ¼W	24773-291S
R54	Met film 1.8kΩ 2% ¼W	24773-279N
R55	Met film 1.8kΩ 2% ¼W	24773-279N
R56	Met film 33kΩ 2% ¼W	24773-309Z
R57	Met film 47kΩ 2% ¼W	24773-313H
R58	Met film 2.4kΩ 2% ¼W	24773-282N
R59	Met film 3.9kΩ 2% ¼W	24773-287V
R60	Met film 56Ω 2% ¼W	24773-243H
TR1	BC239	28452-771P
TR2	BC109	28452-777K
TR3	BCY71	28435-235L
TR4	BC239	28452-771P
TR5	BC107	28455-437L
TR7	BC109	28452-777K
X1	LED/Photocell module PLS-55380M	25687-501B
	37. Unit AS4 - AM and attenuation control	
	Complete board	44828-345Y
C1	Tant 0.47μF 20% 35V	26486-207L
C2	Cer 100pF 2% 100V	26343-477V
C3	Tant 0.47μF 20% 35V	26486-207L
C4	Cer 0.01μF -20+80% 100V	26383-055L
D1	1N4148	28336-676J
D2	LED (Red) TIL220	28624-104W

37. Unit AS4 - AM and attenuation control (continued)

Circuit reference	Description	Code no.
D3	LED (Red) TIL220	28624-104W
IC1	DAC-20CQ	28469-394R
IC2	DAC-20CQ	28469-394R
IC3	μA 741C	28461-304T
RLA	Reed relay RS12V	23486-427A
R1	Met film 4.3kΩ 2% ¼W	24773-288S
R2	Met film 2.4kΩ 2% ¼W	24773-282N
R3	Met film 5.6kΩ 2% ¼W	24773-291S
R4	Met film 5.6kΩ 2% ¼W	24773-291S
R5	Met film 5.6kΩ 2% ¼W	24773-291S
R6	Met film 2.4kΩ 2% ¼W	24773-282N
R7	Met film 2.4kΩ 2% ¼W	24773-282N
R8	Met film 10kΩ 2% ¼W	24773-297M
R9	Met film 27kΩ 2% ¼W	24773-307K
R10	Met film 1kΩ 2% ¼W	24773-273A
R11	Met film 27kΩ 2% ¼W	24773-307K
R12	Met film 1kΩ 2% ¼W	24773-273A
R13	Met film 27kΩ 2% ¼W	24773-307K
R14	Met film 1kΩ 2% ¼W	24773-273A
R15	Met film 27kΩ 2% ¼W	24773-307K
R16	Met film 1kΩ 2% ¼W	24773-273A
R17	Met film 27kΩ 2% ¼W	24773-307K
R18	Met film 1kΩ 2% ¼W	24773-273A
R19	Met film 470kΩ 2% ¼W	24773-337R
R20	Carb 1MΩ 5% 1/8W	24311-945Y
R21	Met film 27kΩ 2% ¼W	24773-307K
R22	Met film 47kΩ 2% ¼W	24773-313H
R23	Met film 330Ω 2% ¼W	24773-261D
R24	Met film 270Ω 2% ¼W	24773-259T
R25	Var cermet 1kΩ 10% ½W	25711-602N
R26	Met film 620Ω 2% ¼W	24773-268B
R27	Met film 100Ω 2% ¼W	24773-249J
SKDT	Con. coaxial 50Ω	23444-334Y
TR1	BC 239C	28452-771P
TR2	BC 239C	28452-771P
TR3	BFY 51	28455-827T
TR4	BC 239C	28452-771P
TR5	BFY 51	28455-827T
TR6	BC 239C	28452-771P
TR7	BFY 51	28455-827T
TR8	BC 239C	28452-771P
TR9	BFY 51	28455-827T
TR10	BC 239C	28452-771P
TR11	BFY 51	28455-827T

Circuit reference	Description	Code no.
	37. Unit AS4 - AM and attenuation control (continued)	
TR12	BC 239C	28452-771P
TR13	BC 239C	28452-771P
TR14	BC 239C	28452-771P
TR15	BC 239C	28452-771P
	38. Unit AS5 - FM control	
	Complete board	44828-346N
C1	Tant 4.7µF 20% 35V	26486-219P
C2	Tant 4.7µF 20% 35V	26486-219P
C3	Cer 10pF ±0.5pF 63V	26343-465H
C4	Cer 10pF ±0.5pF 63V	26343-465H
C5	Cer 10pF ±0.5pF 63V	26343-465H
C6	Plas 0.1µF 10% 100V	26582-211B
C7	Cer 68pF 2% 63V	26343-475F
C8	Cer 68pF 2% 63V	26343-475F
C9	Cer 5.6pF ±0.5pF 63V	26343-462K
C10	Cer 0.01µF -20+100% 40V	26387-253M
C11	Cer 0.01µF -20+100% 40V	26387-253M
C12	Cer 5.6pF ±0.5pF 63V	26343-462K
C13	Cer 0.01µF -20+100% 40V	26387-253M
C14	Cer 0.01µF -20+100% 40V	26387-253M
C15	Cer 100pF 2% 63V	26343-477V
C16	Elec 0.47µF 20% 35V	26486-207L
C17	Elec 0.47µF 20% 35V	26486-207L
C18	Cer 39pF 5% 63V	26343-472N
C19	Cer 0.01µF -20+100% 40V	26387-253M
C20	Tant 4.7µF 20% 35V	26486-219P
C21	Tant 4.7µF 20% 35V	26486-219P
C22	Cer 0.01µF -20+100% 40V	26387-253M
C23	Cer 0.01µF -20+100% 40V	26387-253M
C24	Cer 0.01µF -20+100% 40V	26387-253M
C25	Cer 5.6pF ±0.5pF 63V	26343-462K
C26	Cer 68pF 2% 63V	26343-475F
C27	Cer 0.01µF -20+100% 40V	26387-253M
C28	Cer 0.01µF -20+100% 40V	26387-253M
C29	Cer 100pF 2% 63V	26343-477V
C30	Plas 0.22µF 10% 100V	26582-226G
C31	Plas 0.22µF 10% 100V	26582-226G
C32	Tant 4.7µF 20% 35V	26486-219P
C33	Cer 0.01µF -20+100% 40V	26387-253M
C34	Plas 0.47µF 10% 100V	26582-215H
C35	Cer 22pF 5% 63V	26343-469N
C36	Cer 15pF 5% 63V	26343-467U
C37	Cer 5.6pF ±0.5pF 63V	26343-462K
C38	Cer 0.01µF -20+100% 40V	26387-253M
C39	Cer 100pF 2% 63V	26343-477V
C40	Plas 0.47µF 10% 100V	26582-215H
C41	Elec 100µF -20+100% 25V	26415-813U

38. Unit AS5 - FM control (continued)

Circuit reference	Description	Code no.
C42	Cer 6.8pF ±0.5pF 63V	26343-463A
C43	Cer 22pF 5% 63V	26343-469N
C44	Plas 0.22µF 10% 100V	26582-226G
C45	Cer 0.01µF -20+100% 40V	26387-253M
C46	Elec 4.7µF -20+100% 63V	26415-801M
C47	Tant 4.7µF 20% 35V	26486-219P
C48	Elec 100µF -20+50% 100V	26415-816L
C49	Cer 220pF 2% 63V	26343-481S
C50	Cer 15pF 5% 63V	26343-467U
C51	Cer 22pF 5% 63V	26343-469N
C52	Tant 4.7µF 20% 35V	26486-219P
C53	Tant 4.7µF 20% 35V	26486-219P
C54	Cer 100pF 2% 63V	26343-477V
C55	Plas 0.47µF 10% 100V	26582-215H
C56	Cer 10pF ±0.5pF 63V	26343-465H
C57	Tant 4.7µF 20% 35V	26486-219P
C58	Cer 100pF 2% 63V	26343-477V
C59	Cer 22pF 5% 63V	26343-469N
D1 to D6	1N4148	28336-676J
D7	Z5B20	28372-786A
D8	Z5B18	28372-583Z
D9 to D23	1N4148	28336-676J
D24	Z5B10	28371-843E
D25	Z5B10	28371-843E
IC1	NE5534AH	28461-329V
IC2	NE5534AH	28461-329V
IC3		
IC4	DAC08CQ	28469-395B
IC5	DAC08CQ	28469-395B
IC6	NE 535	28461-343C
IC7 to IC11	NE5534AH	28461-329V
L1	Choke 10µH 10%	23642-555G
RLA	RS12V	23486-427A
RLB	RS12V	23486-427A
RLC	RS12V	23486-427A
RLD	RS12V	23486-427A
RLE	FS2-2A-112	23486-508J
RLF	FS2-2A-112	23486-508J
R1	Var cermet 5kΩ 10% ½W	25711-610V
R2	Var cermet 5kΩ 10% ½W	25711-610V

38. Unit AS5 - FM control (continued)

Circuit reference	Description	Code no.
R3 to R11	Var cermet 10kΩ 10% ½W	25711-603L
R12	Var cermet 2kΩ 10% ½W	25711-609W
R13	Var cermet 2kΩ 10% ½W	25711-609W
R14	Var cermet 200Ω 10% ½W	25711-601Y
R15	Var cermet 500Ω 10% ½W	25711-604J
R16	Var cermet 200Ω 10% ½W	25711-601Y
R17	Var cermet 1MΩ 10% ½W	25711-616X
R18	Var cermet 2kΩ 10% ½W	25711-609W
R19	Var cermet 2kΩ 10% ½W	25711-609W
R20	Var cermet 5kΩ 10% ½W	25711-610V
R21	Met film 390kΩ 2% ¼W	24773-335M
R22	Met film 750Ω 2% ¼W	24773-270R
R23 to R31	Met film 10kΩ 2% ¼W	24773-297M
R32	Met film 12kΩ 2% ¼W	24773-299R
R33	Met film 12kΩ 2% ¼W	24773-299R
R34	Met film 12kΩ 2% ¼W	24773-299R
R35	Carb 10MΩ 5% 1/8W	24321-885W
R36	Carb 10MΩ 5% 1/8W	24321-885W
R37	Carb 10MΩ 5% 1/8W	24321-885W
R38	Met film 2.96kΩ 1% ¼W	24761-988A
R39	Met film 5.96kΩ 1% ¼W	24761-990K
R40	Met film 12kΩ 1% ¼W	24761-806W
R41	Met film 2kΩ 2% ¼W	24773-280U
R42	Met film 1kΩ 2% ¼W	24773-273A
R43	Met film 510Ω 2% ¼W	24773-266C
R44	Met film 510Ω 2% ¼W	24773-266C
R45	Met film 82kΩ 2% ¼W	24773-319J
R46	Met film 130kΩ 2% ¼W	24773-324G
R47	Met film 110kΩ 2% ¼W	24773-322J
R48	Met film 110kΩ 2% ¼W	24773-322J
R49	Met film 1kΩ 2% ¼W	24773-273A
R50	Carb 1MΩ 5% 1/8W	24311-945Y
R51	Carb 1MΩ 5% 1/8W	24311-945Y
R52	Met film 10kΩ 2% ¼W	24773-297M
R53	Met film 10kΩ 2% ¼W	24773-297M
R54	Met film 100Ω 2% ¼W	24773-249J
R55	Met film 5.1kΩ 2% ¼W	24773-290V
R56	Met film 3kΩ 1% ¼W	24761-871V
R57	Met film 10kΩ 1% ¼W	24761-825E
R58	Met film 2.4kΩ 2% ¼W	24773-282N
R59	Met film 10kΩ 1% ¼W	24761-825E
R60	Met film 10kΩ 2% ¼W	24773-297M
R61	Met film 12kΩ 1% ¼W	24761-806W
R62	Met film 3kΩ 1% ¼W	24761-871V

38. Unit AS5 - FM control (continued)

Circuit reference	Description	Code no.
R63	Met film 3kΩ 1% ¼W	24761-871V
R64	Met film 5.1kΩ 2% ¼W	24773-290V
R65	Met film 5.1kΩ 2% ¼W	24773-290V
R66	Met film 5.1kΩ 2% ¼W	24773-290V
R67	Met film 1kΩ 1% ¼W	24761-844P
R68	Met film 3.16kΩ 1% ¼W	24761-989Z
R69	Met film 10kΩ 1% ¼W	24761-825E
R70	Met film 31.6kΩ 1% ¼W	24761-991A
R71	Met film 16kΩ 2% ¼W	24773-302X
R72	Met film 820Ω 2% ¼W	24773-271B
R73	Met film 12kΩ 2% ¼W	24773-299R
R74	Met film 100Ω 2% ¼W	24773-249J
R75	Met film 2kΩ 2% ¼W	24773-280U
R76	Met film 13kΩ 2% ¼W	24773-300T
R77	Met film 2kΩ 2% ¼W	24773-280U
R78	Met film 1.3kΩ 2% ¼W	24773-276E
R79	Met film 4.3kΩ 2% ¼W	24773-288S
R80	Met film 1kΩ 2% ¼W	24773-273A
R81	Met film 12kΩ 2% ¼W	24773-299R
R82	Met film 100Ω 2% ¼W	24773-249J
R83	Met film 100kΩ 2% ¼W	24773-321L
R84	Met film 510Ω 2% ¼W	24773-266C
R85	Met film 510Ω 2% ¼W	24773-266C
R86	Met film 3.3kΩ 2% ¼W	24773-285F
R87	Met film 22kΩ 2% ¼W	24773-305R
R88	Met film 68kΩ 2% ¼W	24773-317N
R89	Met film 3.9kΩ 2% ¼W	24773-287V
R90	Met film 2kΩ 2% ¼W	24773-280U
R91	Met film 68kΩ 2% ¼W	24773-317N
R92	Met film 390Ω 2% ¼W	24773-263P
R93	Met film 51Ω 2% ¼W	24773-242Z
R94	Met film 51Ω 2% ¼W	24773-242Z
R95	Met film 100Ω 2% ¼W	24773-249J
R96	Met film 220Ω 2% ¼W	24773-257W
R97	Met film 3.3kΩ 2% ¼W	24773-285F
R98	Met film 620Ω 2% ¼W	24773-268B
R99	Met film 3.6kΩ 2% ¼W	24773-286G
R100	Met film 680Ω 2% ¼W	24773-269K
R101	Met film 2.7kΩ 2% ¼W	24773-283L
R102	Met film 680Ω 2% ¼W	24773-269K
R103	Met film 30kΩ 2% ¼W	24773-308A
R104	Met film 11kΩ 2% ¼W	24773-298C
R105	Met film 4.7kΩ 2% ¼W	24773-289W
R106	Met film 20kΩ 2% ¼W	24773-304C
R107	Met film 6.2kΩ 2% ¼W	24773-292W
R108 to R116	Met film 1.5kΩ 2% ¼W	24773-277U

38. Unit AS5 - FM control (continued)

Circuit reference	Description	Code no.
R117	Met film 4.7kΩ 2% ¼W	24773-289W
R118	Met film 2kΩ 2% ¼W	24773-280U
R119	Met film 2kΩ 2% ¼W	24773-280U
R120	Met film 4.7kΩ 2% ¼W	24773-289W
R121	Met film 4.7kΩ 2% ¼W	24773-289W
R122	Met film 4.7kΩ 2% ¼W	24773-289W
R123	Met film 1kΩ 2% ¼W	24773-273A
R124	Met film 750Ω 2% ¼W	24773-270R
R125	Met film 3kΩ 2% ¼W	24773-284J
R126	Met film 1kΩ 2% ¼W	24773-273A
R127	Met film 4.7kΩ 2% ¼W	24773-289W
R128 †	Met film 220Ω 2% ¼W	24773-257W
R129	Carb 1MΩ 5% 1/8W	24311-945Y
R130	Carb 1MΩ 5% 1/8W	24311-945Y
R131	Met film 1kΩ 2% ¼W	24773-273A
R132	Met film 43kΩ 2% ¼W	24773-312Z
R133	Met film 43kΩ 2% ¼W	24773-312Z
R134	Met film 43kΩ 2% ¼W	24773-312Z
R135 †	Met film 220Ω 2% ¼W	24773-257W
R136	Met film 3kΩ 2% ¼W	24773-284J
R137	Met film 100Ω 2% ¼W	24773-249J
R138	Met film 100Ω 2% ¼W	24773-249J
R139	Met film 68kΩ 2% ¼W	24773-317N
R140	Met film 100kΩ 2% ¼W	24773-321L
R141	Met film 16kΩ 2% ¼W	24773-302X
R142	Met film 100Ω 2% ¼W	24773-249J
R143	Met film 39kΩ 2% ¼W	24773-311A
R144	Met film 5.1kΩ 2% ¼W	24773-290V
R145	Met film 20kΩ 2% ¼W	24773-304C
SKBN	Con. coaxial	23444-334Y
TR1	BC 239C	28452-771P
TR2	BC 239C	28452-771P
TR3	BC 239C	28452-771P
TR4	BCY 71	28435-235L
TR5	BCY 71	28435-235L
TR6	BCY 71	28435-235L
TR7	J310	28459-028E
TR8	J310	28459-028E
TR9	J310	28459-028E
TR10	E431	28459-034N
TR11 to TR14	BC 239C	28452-771P
TR15	2N2219	28453-847F
TR16	BCY 71	28435-235L
TR17	BCY 71	28435-235L

Circuit reference	Description	Code no.
	38. Unit AS5 - FM control (continued)	
TR18	MM4001	28438-436V
TR19	BC 237A	28455-421X
TR20	BF 338	28458-577X
TR21	BF 338	28458-577X
TR22	MM 4001	28438-436V
TR23	BC 237A	28455-421X
TR24	BC 237A	28455-421X
TR25 to TR34	BCY 71	28435-235L
TR35	BC 239C	28452-771P
	39. Unit AK4 - Modulation oscillator	
	Complete assy.	44990-303Z
R3	Var cermet Inv. Log. 25kΩ x 25kΩ	25741-102C
	40. Unit AK4A - Modulation oscillator switch board	
	Complete board	44828-353G
C1	Plas 0.1μF 2% 250V	26582-299P
C2	Plas 0.01μF 2% 250V	26582-297D
C3	Plas 0.001μF 2% 160V	26516-481L
C4	Plas 4.7μF 10% 63V	26582-421Z
C5	Plas 0.47μF 2% 63V	26582-409M
C6	Plas 0.047μF 10% 250V	26582-206C
C9	Plas 0.033μF 2% 250V	26582-298T
C10	Plas 0.0033μF 2% 160V	26516-609Z
C11	Plas 330pF 2% 350V	26516-372E
SA	6 pos. 4 pole	23462-076A
R1	Met film 10kΩ 1% ¼W	24761-825E
R2	Met film 4.02kΩ 1% ¼W	24761-960Z
R4	Met film 1.8kΩ 2% ¼W	24773-279N
R5	Met film 10kΩ 1% ¼W	24761-825E
R7	Met film 4.02kΩ 1% ¼W	24761-960Z
R9	Met film 1.8kΩ 2% ¼W	24773-279N

Circuit reference	Description	Code no.
	41. Unit AK4B - Modulation oscillator rear board	
	Complete board	44828-354V
C12	Cer 0.001μF 10% 63V	26383-585M
C13	Cer 330pF 2% 350V	26383-597U
C14	Tant 4.7μF 20% 35V	26486-219P
C15	Tant 4.7μF 20% 35V	26486-219P
C16	Cer 47pF 5% 63V	26343-473L
C17	Cer 22pF 5% 63V	26343-469N
D1	1N4148	28336-676J
D2	1N4148	28336-676J
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	Z5B 5.6	28371-434Y
IC1	74LS03	28466-346E
IC2	NE 535	28461-343C
IC3	NE 5534AH	28461-329V
IC4	NE 535	28461-343C
R10	Met film 2.2kΩ 2% ¼W	24773-281Y
R11	Met film 27kΩ 2% ¼W	24773-307K
R12	Met film 100kΩ 2% ¼W	24773-321L
R13	Carb 1MΩ 5% 1/8W	24311-945Y
R14	Met film 6.2kΩ 2% ¼W	24773-292W
R15	Met film 62kΩ 2% ¼W	24773-316Y
R16	Met film 470Ω 2% ¼W	24773-265M
R17	Met film 2.7kΩ 2% ¼W	24773-283L
R18	Var cermet 500Ω 10% ½W	25711-604J
R19	Met film 100kΩ 2% ¼W	24773-321L
TR1	BCY 70	28434-857Z
TR2	J 310	28459-028E
X1	Cadmium sulphide opto coupler	25687-530M
	42. Unit AT0 - Attenuator assembly	
	Complete assy.	44990-304H
	Solenoid assy. RLA-F	44990-150D
D1 to D6	1N4148	28336-676J
PLCV	10-way	23435-019V
SKCT	Bulkhead receptacle	23444-382T
SKCU	Bulkhead jack (SRM 50-647-0000-31)	23444-510N
	43. Unit AT1 - Attenuator board	
	Complete board	44828-355S
R1	Chip 53.3Ω 1% 100V	24681-023S

Circuit reference	Description	Code no.
	43. Unit AT1 - Attenuator board (continued)	
R2	Chip 790Ω 1% 100V	24681-033C
R3	Chip 53.3Ω 1% 100V	24681-023S
R4	Chip 53.3Ω 1% 100V	24681-023S
R5	Chip 790Ω 1% 100V	24681-033C
R6	Chip 53.3Ω 1% 100V	24681-023S
R7	Chip 83.5Ω 1% 100V	24681-038Z
R8	Chip 93.2Ω 1% 100V	24681-039H
R9	Chip 83.5Ω 1% 100V	24681-038Z
R10	Chip 53.3Ω 1% 100V	24681-023S
R11	Chip 790Ω 1% 100V	24681-033C
R12	Chip 53.3Ω 1% 100V	24681-023S
R13	Chip 150.5Ω 1% 100V	24681-040A
R14	Chip 37.3Ω 1% 100V	24681-036K
R15	Chip 150.5Ω 1% 100V	24681-040A
R16	Chip 56.7Ω 1% 100V	24681-037A
R17	Chip 394Ω 1% 100V	24681-041Z
R18	Chip 56.7Ω 1% 100V	24681-037A
SA to SN	Microswitch SPDT	23483-144G

Circuit reference	Description	Code no.
	44. Unit AR0 - Reverse power protection	
	Complete assy.	44990-305E
C1 Ø	Cer 10pF ±1pF 300V	26333-228E
C2 Ø	Cer 10pF ±1pF 300V	26333-228E
C3 Ø	Cer 50pF 10% 300V	26333-229U
C4 Ø	Cer 50pF 10% 300V	26333-229U
C5 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C6 Ø	Cer 0.001μF -20+80% 300V	26373-733K
C7 Ø	Cer 0.001μF -20+80% 300V	26373-733K
RLA	Coil assy.	44290-750K
	Reed switch	23486-452P
	45. Unit AR1A - RPP detector	
	Complete board	44828-603T
C21	Cer 0.1μF -20+80% 50V	26386-496S
C22	Cer 0.1μF -20+80% 50V	26386-496S
D1	HP 5082-2800	28349-007E
D2	HP 5082-2811	28349-008U
D3	HP 5082-2800	28349-007E
D4	HP 5082-2811	28349-008U
D5	Z5B 10	28371-843E
D6	1N4148	28336-676J
D7	Z5B 24	28373-271J

Circuit reference	Description	Code no.
	45. Unit AR1A - RPP detector (continued)	
R2	Carb 10MΩ 5% 1/8W	24331-955D
R3	Carb 10MΩ 5% 1/8W	24331-955D
R4	Carb 10MΩ 5% 1/8W	24331-955D
R21	Chip 470Ω 5%	24681-046N
R22	Chip 470Ω 5%	24681-046N
R23	Chip 220Ω 5%	24681-049F
R24	Chip 220Ω 5%	24681-049F
	46. Unit AR1B - RPP control	
	Complete board	44828-363X
C2	Cer 3.3pF ±0.5pF 63V	26343-459K
C3	Cer 220pF 10% 63V	26383-595H
C6	Cer 33pF 5% 63V	26343-471Y
C7	Cer 68pF 2% 63V	26343-475F
IC1	TL081CP	28461-335D
IC2	MLM311P1	28461-695U
R4	Carb film 10MΩ 10% 1/8W	24321-885W
R6	Carb film 10MΩ 10% 1/8W	24321-885W
R7	Met film 10kΩ 2% ¼W	24773-297M
R8	Met film 3.3kΩ 2% ¼W	24773-285F
R9	Var cermet 2kΩ 10% ½W	25711-609W
R10	Met film 8.2kΩ 2% ¼W	24773-295P
R11	Met film 4.7kΩ 2% ¼W	24773-289W
R12	Met film 10kΩ 2% ¼W	24773-297M
R13	Met film 10kΩ 2% ¼W	24773-297M
R14	Met film 47kΩ 2% ¼W	24773-313H
R15	Met film 47kΩ 2% ¼W	24773-313H
R16	Met film 10kΩ 2% ¼W	24773-297M
R17	Met film 22kΩ 2% ¼W	24773-305R
R18	Met film 15kΩ 2% ¼W	24773-301P
TR1	2N2219	28453-847F
TR2	BCY 70	28434-857Z
TR3	BC 239C	28452-771P
TR4	BC 239C	28452-771P
	47. Unit AS6 - Manual/motor connector board	
	Complete board	44828-347L
	48. Unit AS7 - VCO steering and motor drive	
	Complete assy.	44990-302A
	49. Unit AS7A - VCO steering	
	Complete board	44828-348J
C1	Tant 4.7μF 20% 35V	26486-219P
C2	Cer 100pF 2% 63V	26343-477V
C3	Tant 4.7μF 20% 35V	26486-219P
C4	Cer 0.47μF 20% 35V	26486-207L

Circuit reference	Description	Code no.
	49. Unit AS7A - VCO steering (continued)	
C5	Tant 4.7μF 20% 35V	26486-219P
C6	Tant 4.7μF 20% 35V	26486-219P
C7	Tant 4.7μF 20% 35V	26486-219P
D2	Z5B13	28372-213U
IC1	μA741C	28461-304T
IC2	μA723C	28461-706F
IC3	μA741C	28461-304T
IC4	μA741C	28461-304T
R1	Met film 1.5kΩ 2% ¼W	24773-277U
R2	Met film 10Ω 2% ¼W	24773-225W
R3	Met film 2.4kΩ 2% ¼W	24773-282N
R4	Met film 3.6kΩ 2% ¼W	24773-286G
R5	Var cermet 1kΩ 10% ½W	25711-602N
R6	Met film 390Ω 2% ¼W	24773-263P
R7	Met film 4.7kΩ 2% ¼W	24773-289W
R8	Met film 6.2kΩ 2% ¼W	24773-292W
R9	Var cermet 1kΩ 10% ½W	25711-602N
R10	Met film 3.3kΩ 2% ¼W	24773-285F
R12	Met film 470kΩ 2% ¼W	24773-337R
R13	Met film 33Ω 2% ¼W	24773-237K
R14	Met film 10kΩ 2% ¼W	24773-297M
R15	Met film 10kΩ 2% ¼W	24773-297M
R16 †	Met film 11kΩ 2% ¼W	24773-298C
R17 †	Met film 3.9kΩ 2% ¼W	24773-287V
R18 †	Met film 1MΩ 2% ¼W	24773-346E
R19 †	Met film 8.2kΩ 2% ¼W	24773-295P
R20	Met film 10kΩ 2% ¼W	24773-297M
TR1	BC308B	28433-455R
TR2	BC239C	28452-771P
TR3	J310	28459-028E
	50. Unit AS7B - VCO moto. drive	
	Complete board	44828-349F
C8	Tant 4.7μF 20% 35V	26486-219P
C9	Cer 0.01μF -20+100% 40V	26387-253M
C10	Cer 0.01μF -20+100% 40V	26387-253M
C11	Elec 100μF -20+100% 25V	26415-813U
C12	Cer 0.022μF -20+80% 18V	26383-007R
C13	Cer 0.01μF -20+100% 40V	26387-253M
C14	Cer 0.022μF -20+80% 18V	26383-007R
C15	Tant 0.4μF 20% 35V	26486-207L
D3	1N4148	28336-676J
D4	1N4148	28336-676J
D5	1N4004	28357-028K
IC5	74LS04	28469-171L

Circuit reference	Description	Code no.
	50. Unit AS7B - VCO motor drive (continued)	
IC6	74LS10	28466-351Y
IC7	μA741C	28461-304T
RLA	RS-12V	23486-427A
RLV	RS-12V	23486-427A
R21	Met film 10Ω 2% ¼W	24773-225W
R22	Met film 22kΩ 2% ¼W	24773-305R
R23	Met film 68kΩ 2% ¼W	24773-317N
R24	Met film 10kΩ 2% ¼W	24773-297M
R25	Met film 10kΩ 2% ¼W	24773-297M
R26	Met film 10kΩ 2% ¼W	24773-297M
R27	Met film 3.3kΩ 2% ¼W	24773-285F
R28	Met film 2.7kΩ 2% ¼W	24773-283L
R29	Met film 510Ω 2% ¼W	24773-266C
R30	Met film 1.8kΩ 2% ¼W	24773-279N
R31	Met film 620Ω 2% ¼W	24773-268B
R32	Met film 3.3kΩ 2% ¼W	24773-285F
R33	Met film 3.3kΩ 2% ¼W	24773-285F
R34	Met film 47kΩ 2% ¼W	24773-313H
R35	Var cermet 10kΩ 10% ½W	25711-603L
R36	Met film 47kΩ 2% ¼W	24773-313H
R37	Met film 120kΩ 2% ¼W	24773-323F
R38	Met film 100Ω 2% ¼W	24773-249J
R39	Met film 120kΩ 2% ¼W	24773-323F
R40	Met ox 15Ω 2% ½W	24573-029L
R41	Met film 1kΩ 2% ¼W	24773-273A
R42	Met film 3.3Ω 2% ¼W	24773-213U
TR4	BC 239C	28452-771P
TR6	BC 239C	28452-771P
TR7	BC 239C	28452-771P
TR8	BC 239C	28452-771P
TR9	BC 239C	28452-771P
TR10	BFY 51	28455-827T
TR11	BC 239C	28452-771P

Circuit reference	Description	Code no.
	MECHANICAL COMPONENTS	
Fig. 1 Item	51. Order without prefix.	
1	Display panel	37590-305Y
2	Front panel	35902-814B
3	Knob assy.	41149-055G
	Cap 20 mm dia.	37590-281W
4	Knob assy.	41149-057S
	Cap 32 mm dia.	37590-282D
	Cap 9 mm dia.	37590-278W
5	Knob assy.	41149-047Y
	Cap 10.5 mm dia.	37590-242F
6	Front foot moulding	37590-253X
7	Knob assy.	41149-048N
	Cap 10.5 mm dia.	37590-242F
8	Socket, bulkhead BNC 50Ω	23443-446H
9	Front panel switch caps, marked :-	
	% dB	37590-306N
	MHz/V	37590-307L
	kHz/mV	37590-308J
	Hz/μV	37590-309F
	OFF/ON	37590-310L
	ON/OFF	37590-311J
	UNLOCK/LOCK	37590-312F
	ROTARY	37590-313G
	EXT	37590-314V
	RETURN/LOCAL	37590-315S
	TOTAL SHIFT	37590-316W
	CARRIER FREQ	37590-317D
	FM DEVIATION	37590-318T
	AM DEPTH	37590-319P
	RF LEVEL	37590-320D
	△ F/SWEEP OFF	37590-321T
	SWEEP	37590-322P
	STORE	37590-323X
	RECALL	37590-324M
	0	37590-325C
	(·)	37590-326R
	(-)	37590-327B
	(1)	37590-328K
	(2)	37590-329A
	(3)	37590-330B
	(4)	37590-331K
	(5)	37590-332A
	(6)	37590-333Z
	(7)	37590-334H
	(8)	37590-335E
	(9)	37590-336U
	UP	37590-337Y
	DOWN	37590-338N
10	Knob assy.	41149-055G
	Knob assy.	41149-050Y
	Cap 14.5 mm dia.	37590-279D

MECHANICAL COMPONENTS (continued)

Circuit reference	Description	Code no.
Fig. 1 Item		
11	RF output socket 'N' type 50Ω	23443-769W
12	Knob assy.	41149-054F
	Cap 14.5 mm dia.	37590-279D
13	Knob assy.	41149-054F
	Cap 14.5 mm dia.	37590-279D
14	Knob assy.	41149-052L
	Cap 14.5 mm dia.	37590-279D
15	Top cover	35902-831F
16	Front Top/Bottom trim	34900-477G
	Plastic trim strip	35902-371Z
17	Logic box cover	41690-267V
18	Rear trim	34900-470E
19	Blanking plug (RF OUT 50Ω)	23188-254B
20	24-way socket (SKR, GPIB)	23435-133X
21	Switch 6 position (GPIB CONTROL)	23467-310C
22	Filter cover	35902-837T
	Air filter	37490-431W
	Fan seal	37490-493V
	Anti-vibration mount	22773-580H
23	Rear foot	37590-224R
	Stud	37590-223C
24	Power supply plug, includes connector/mains filter	23423-150L
25	INT/EXT STD switch (SBC)	23462-252Z
26	Socket, bulkhead BNC 50Ω	23443-446H
27	End cap cover moulding	37590-256R
28	Rear panel	35902-916B
29	Bottom cover	35902-832G
30	Cap and chain BNC	23443-592V
31	Side panel LH	35902-914C
	Side panel RH	35902-915R
32	Side rail	34900-476F
	Plastic trim strip	35902-386W
33	Steel liner 2 off	22315-587M
34	PVC extrusion	22315-590M
35	Liner	22315-584T
36	Cover moulding	37590-257B
37	Panel handle	41700-266J
38	Trim plate	35902-369H
39	Bush	33900-665K
40	Support panel assy.	35902-726F

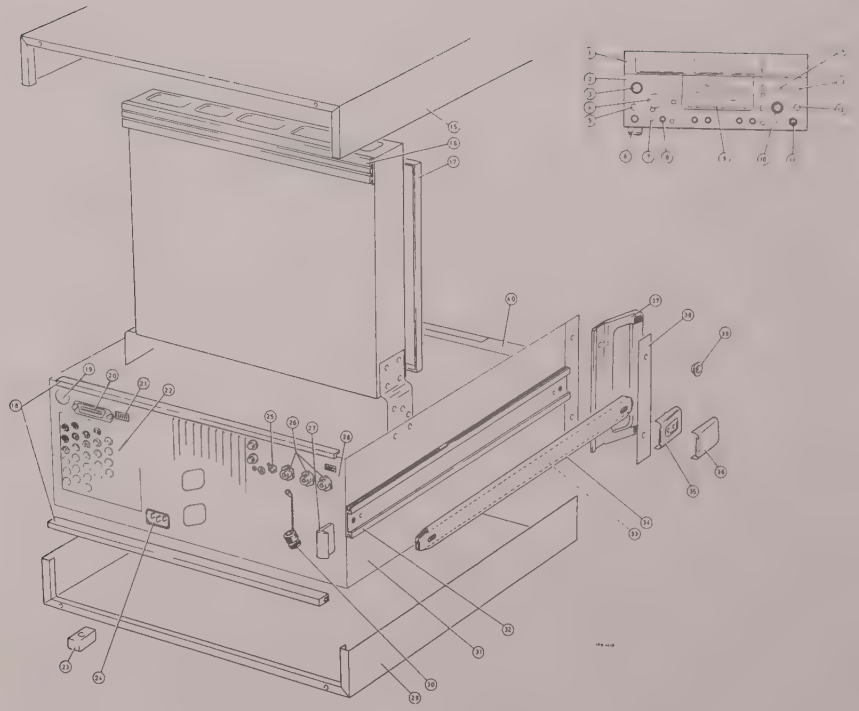

Fig. 1 Miscellaneous mechanical parts

Chapter 7

SERVICING DIAGRAMS

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1 Component values
2 Symbols

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CIRCUIT NOTES

Component values

1. Resistors : No suffix = ohms, k = kilohms, M = megohms.
Capacitors : No suffix = microfarads, p = picofarads.
Inductors : No suffix = henrys, m = millihenrys, μ = microhenrys.
† SIC : value selected during test, nominal value shown.

Symbols

2. Symbols are based on the provisions of BS 3939 with the following additions.

edge connector

ferrite bead

warning, see page (iv), notes and cautions

beryllia : health hazard, see page (iv) notes and cautions.

unit identification number.

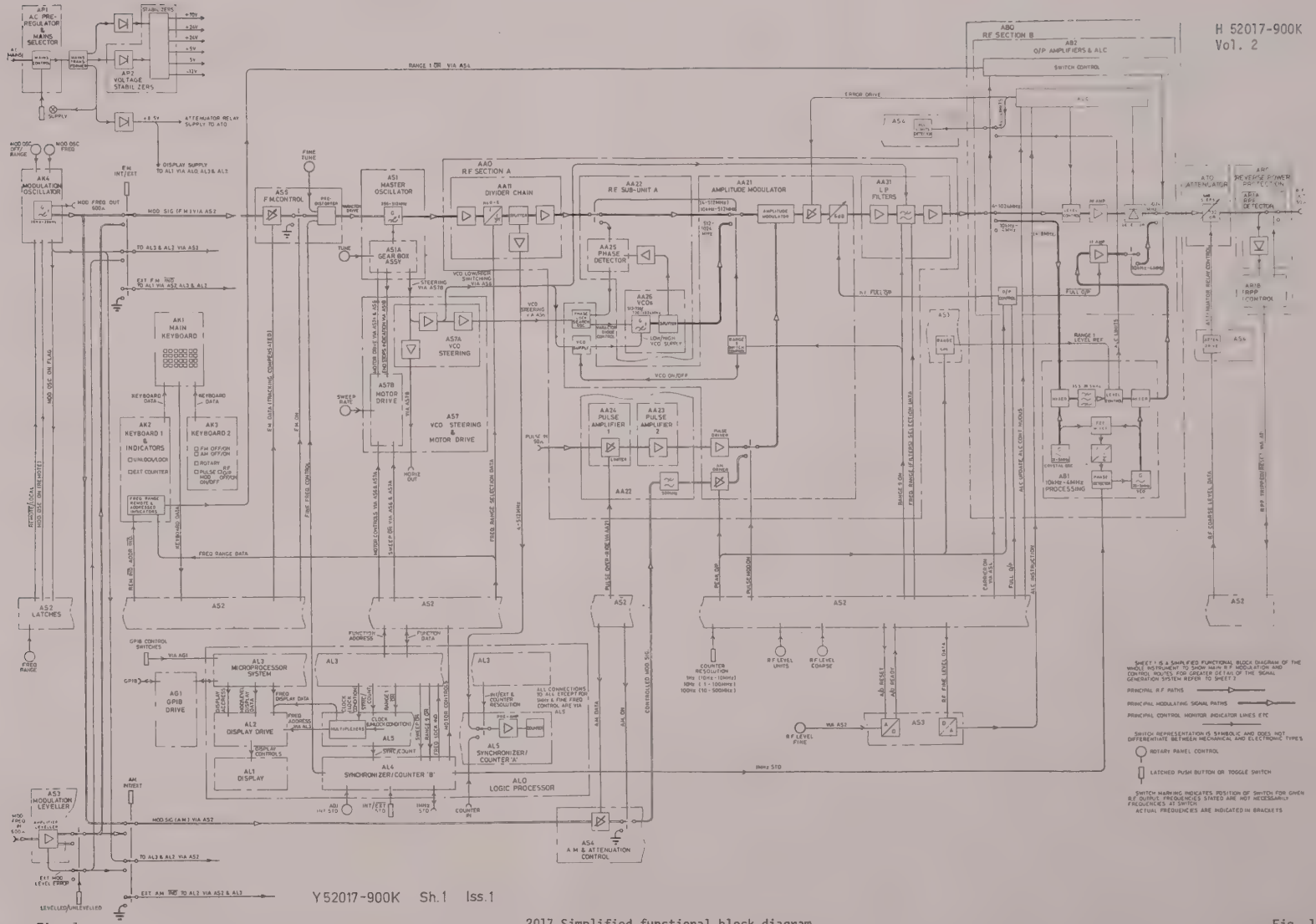

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Fig. 1

2017 Simplified functional block diagram

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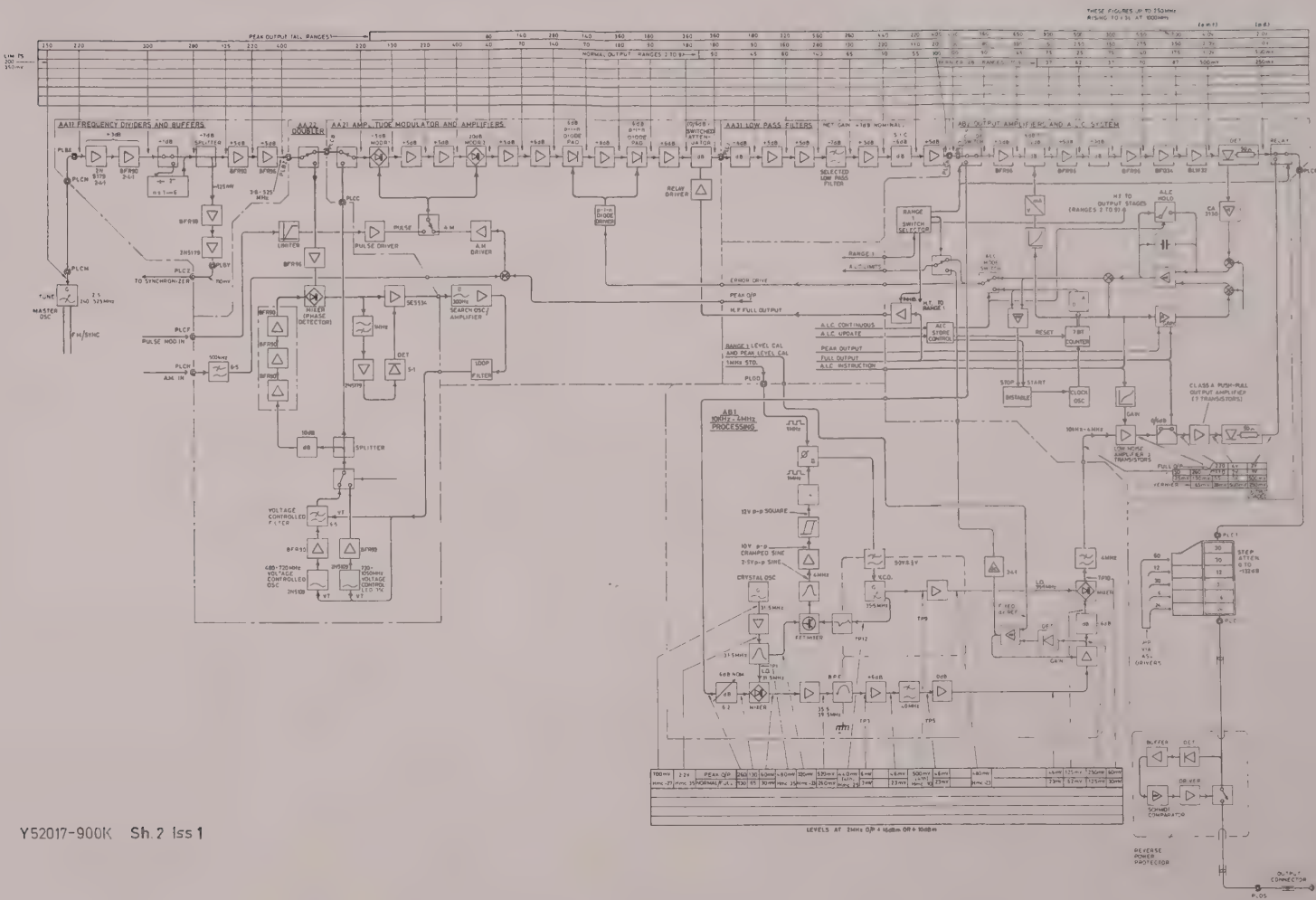

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Fig. 2

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2017 Simplified block diagram showing signal paths and voltage levels

Fig. 2
Chap. 7
Page 5

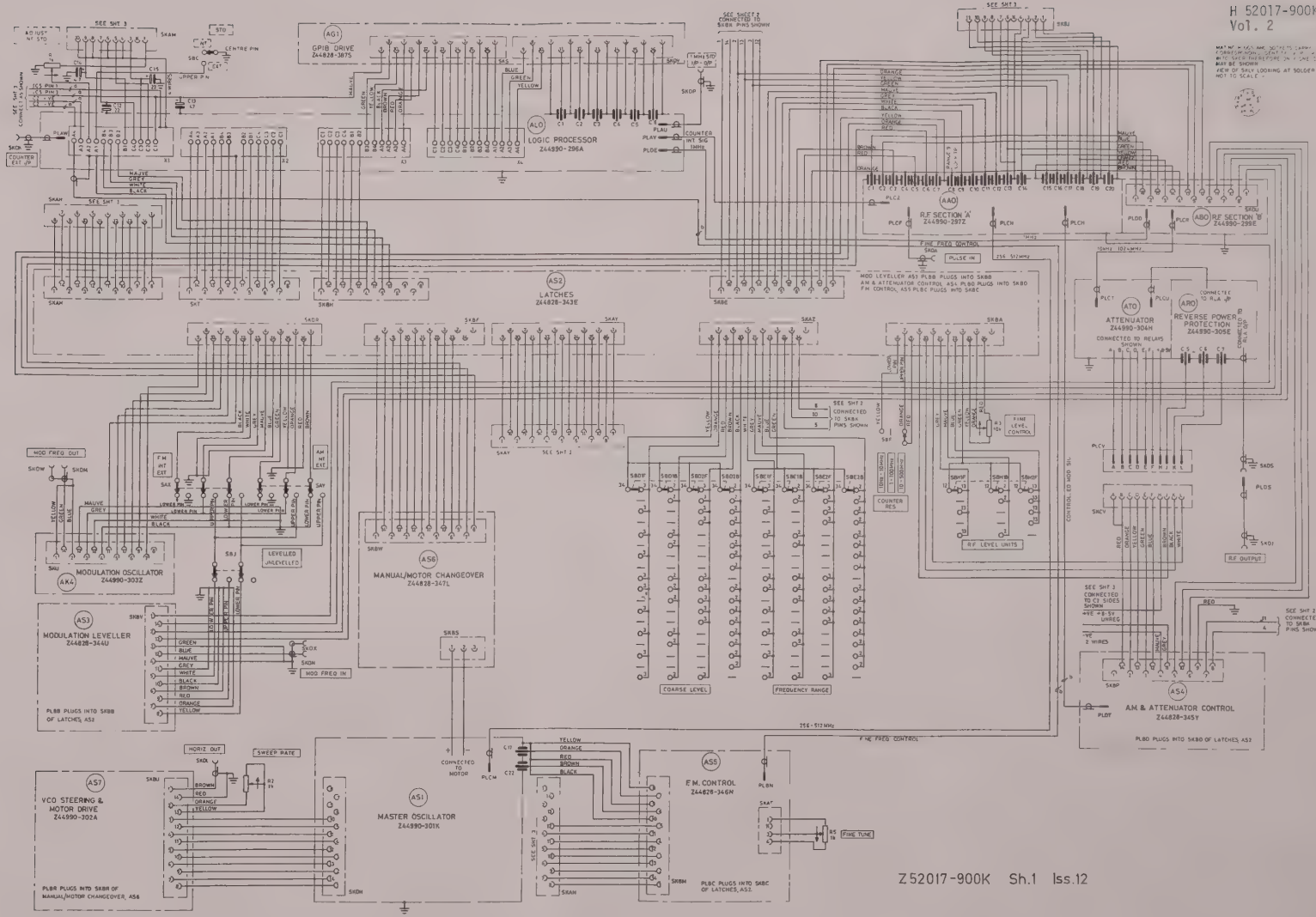

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Fig. 3

Signal Generator 2017 interconnections A0

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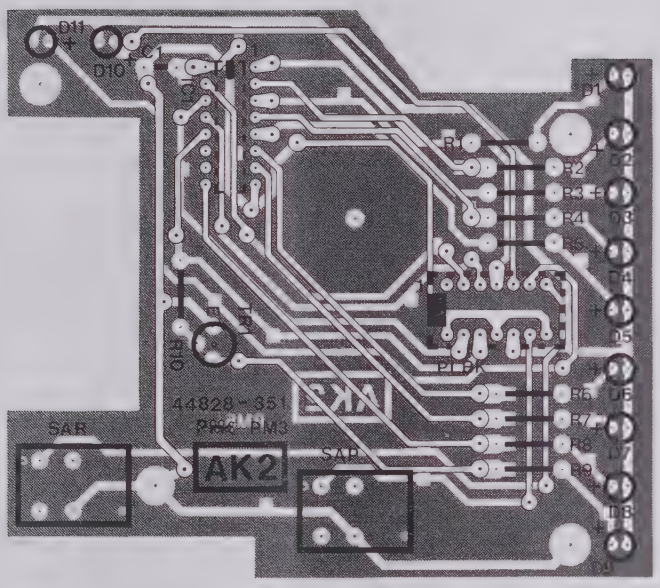

Fig. 4a
Chap. 7
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Component layout, AK2

Fig. 4a

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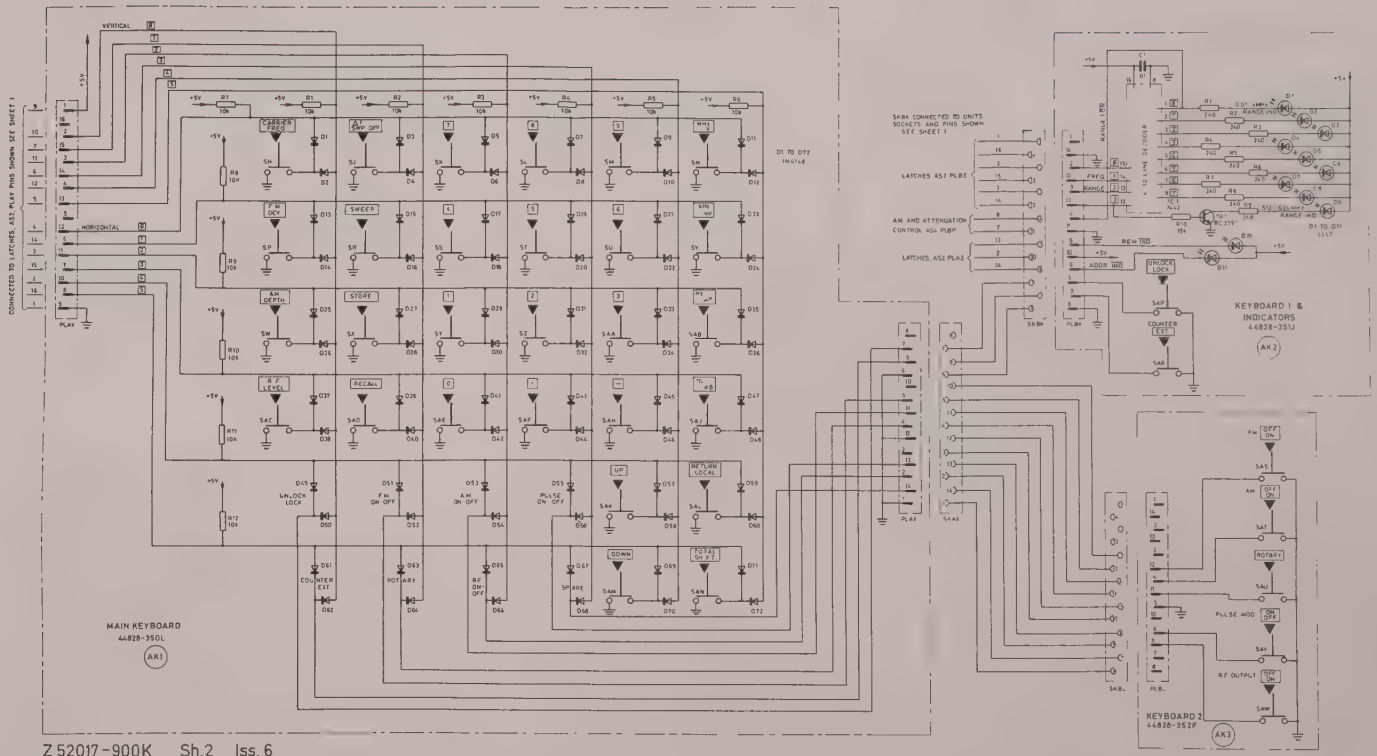

Z 52017-900K Sh.2 Iss.6

Fig. 4

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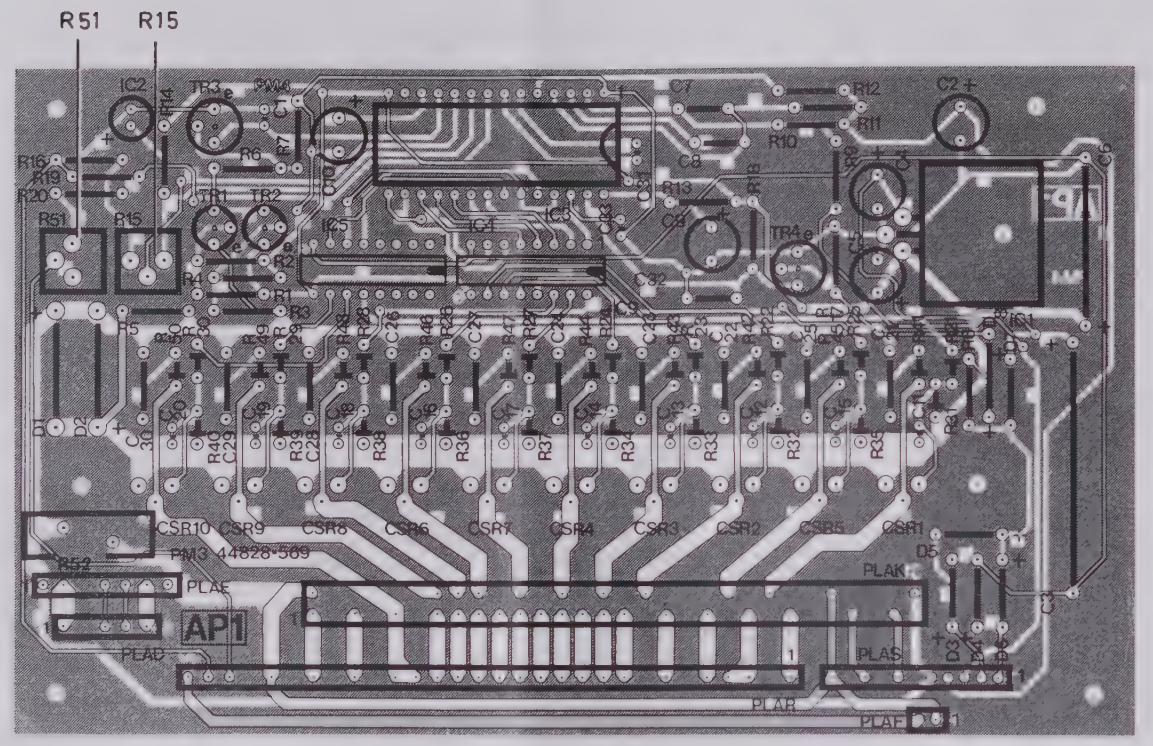
Keyboards AK1, AK2, AK3, circuit diagram

Fig. 4
Chap. 7
Page 9



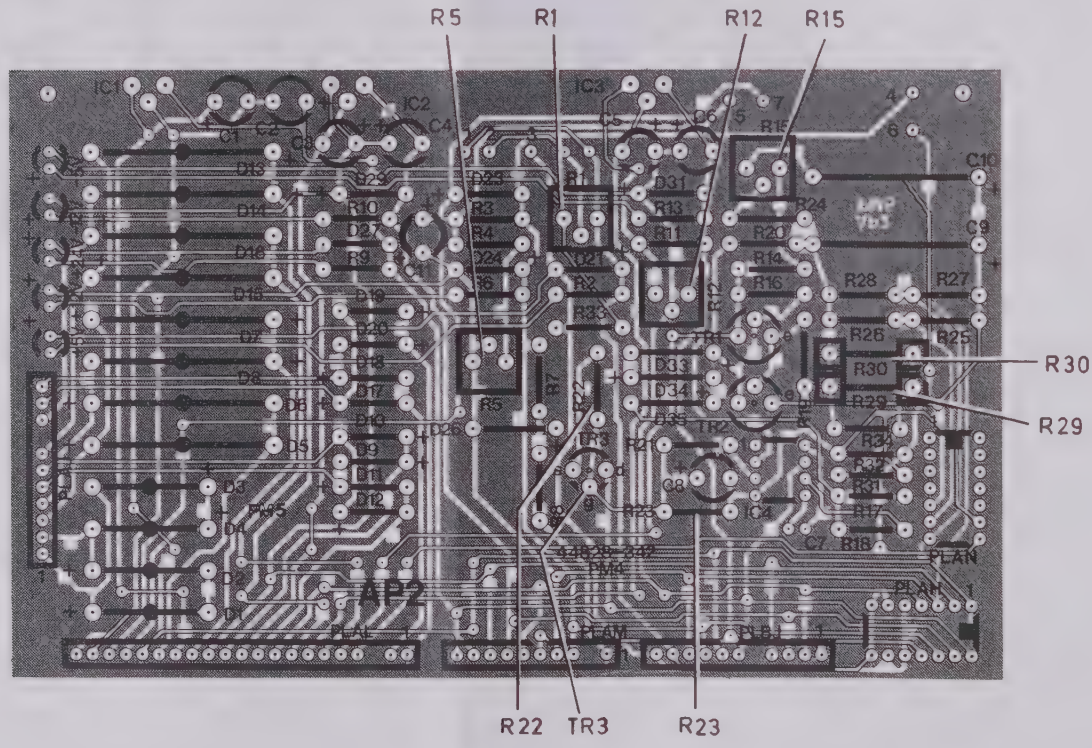


Fig. 5a
Chap. 7
Page 10

Component layout, AP1 and AP2

Fig. 5a

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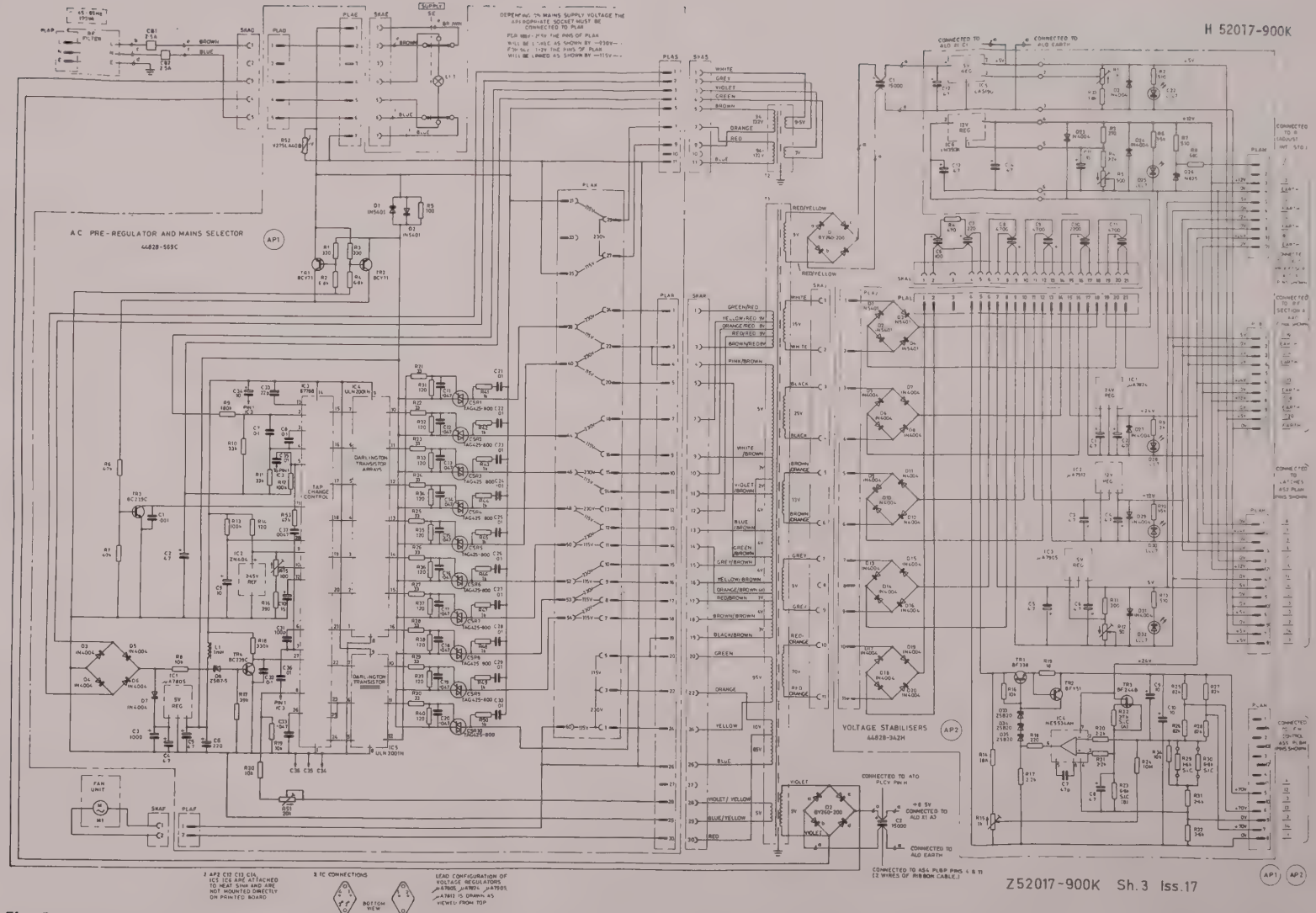

Fig. 5

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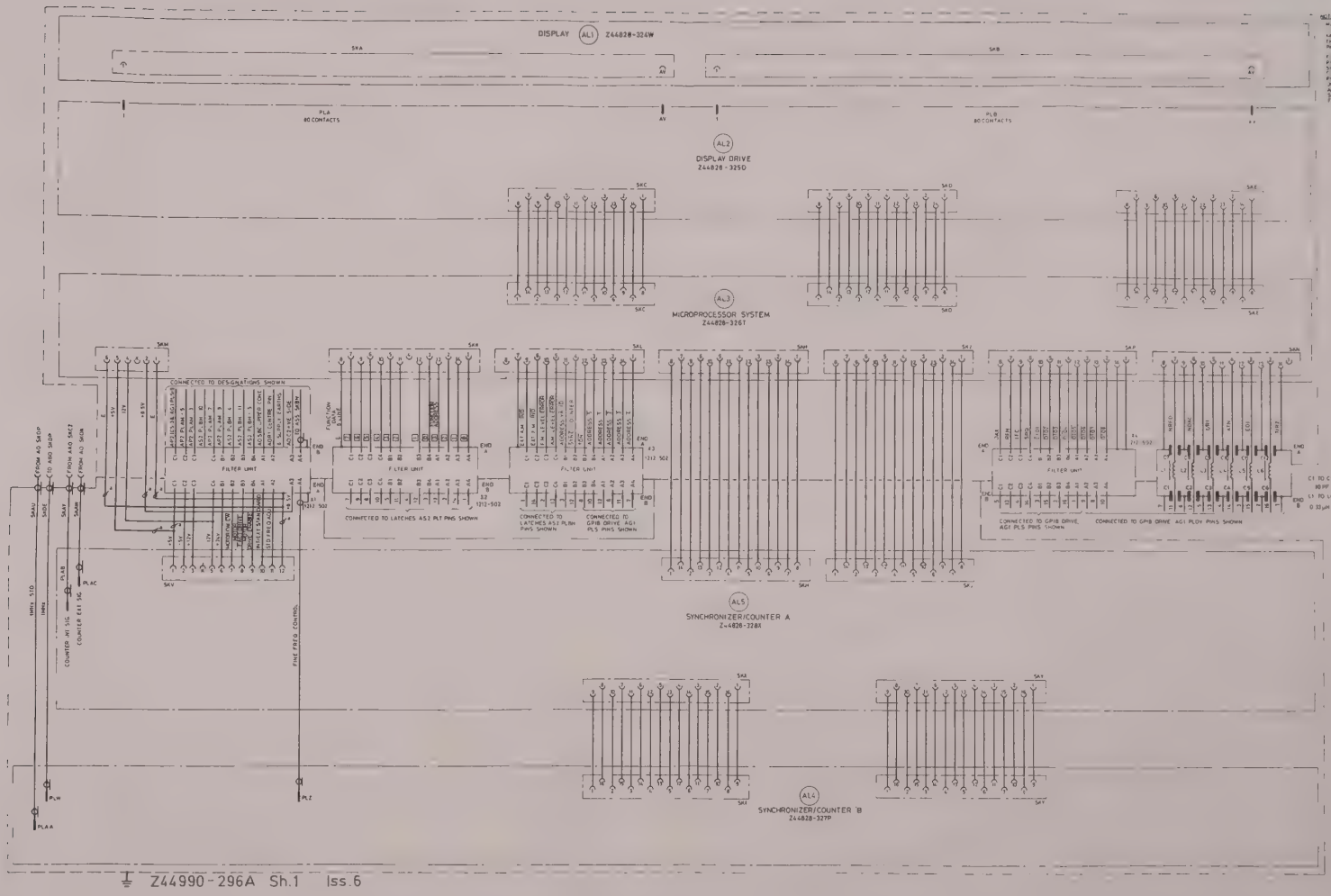
AC pre-regulator and mains selector AP1, voltage stabilizers AP2, circuit diagram A0



Z44990-296A Sh.1 Iss.6

Fig. 6

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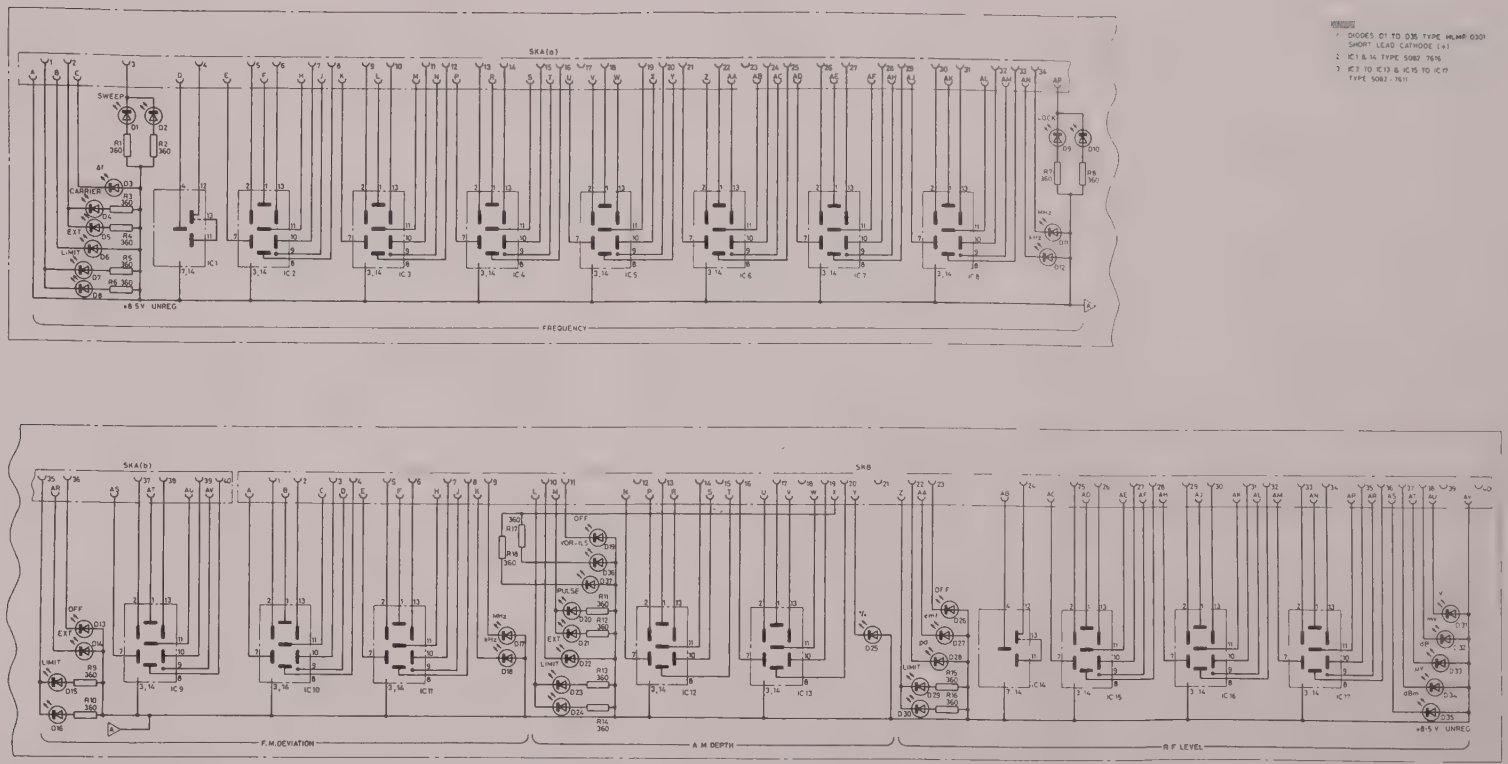
Logic processor interconnections, AL0



Z44828-324W Sh.1 Iss. 5

Fig. 7

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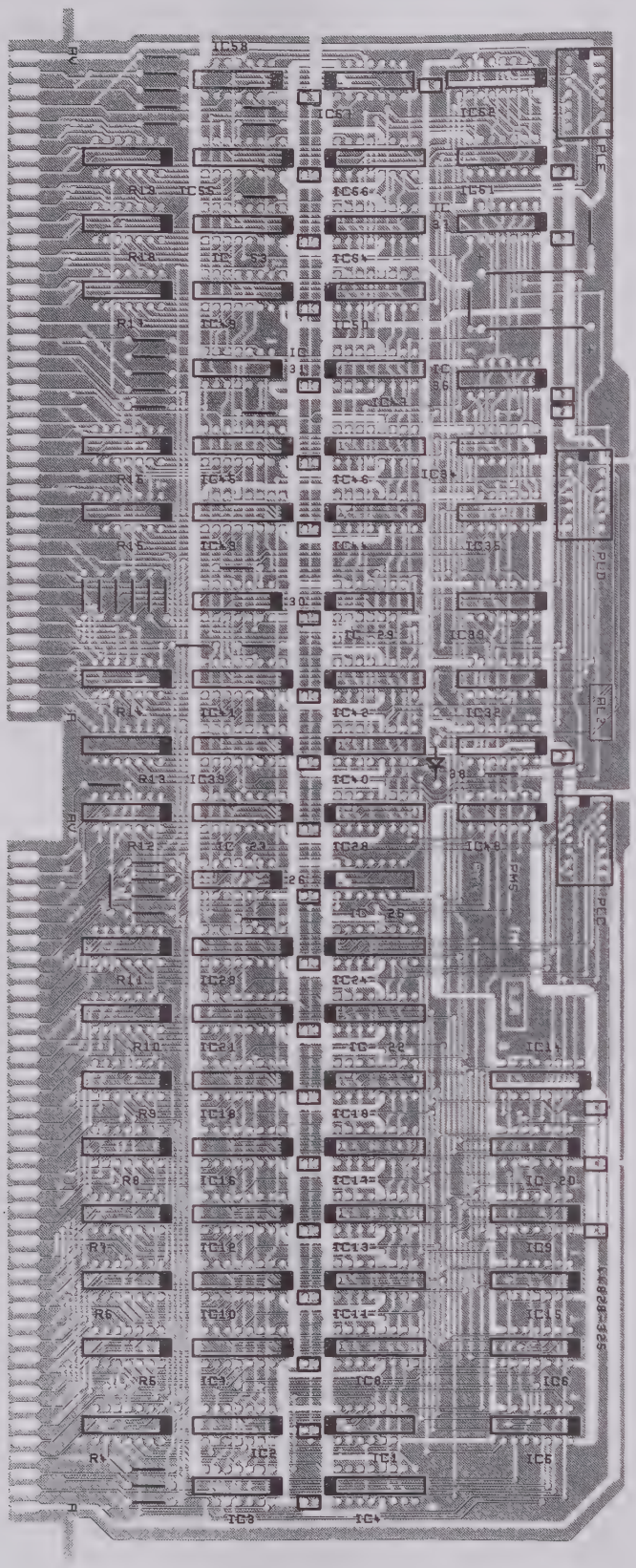
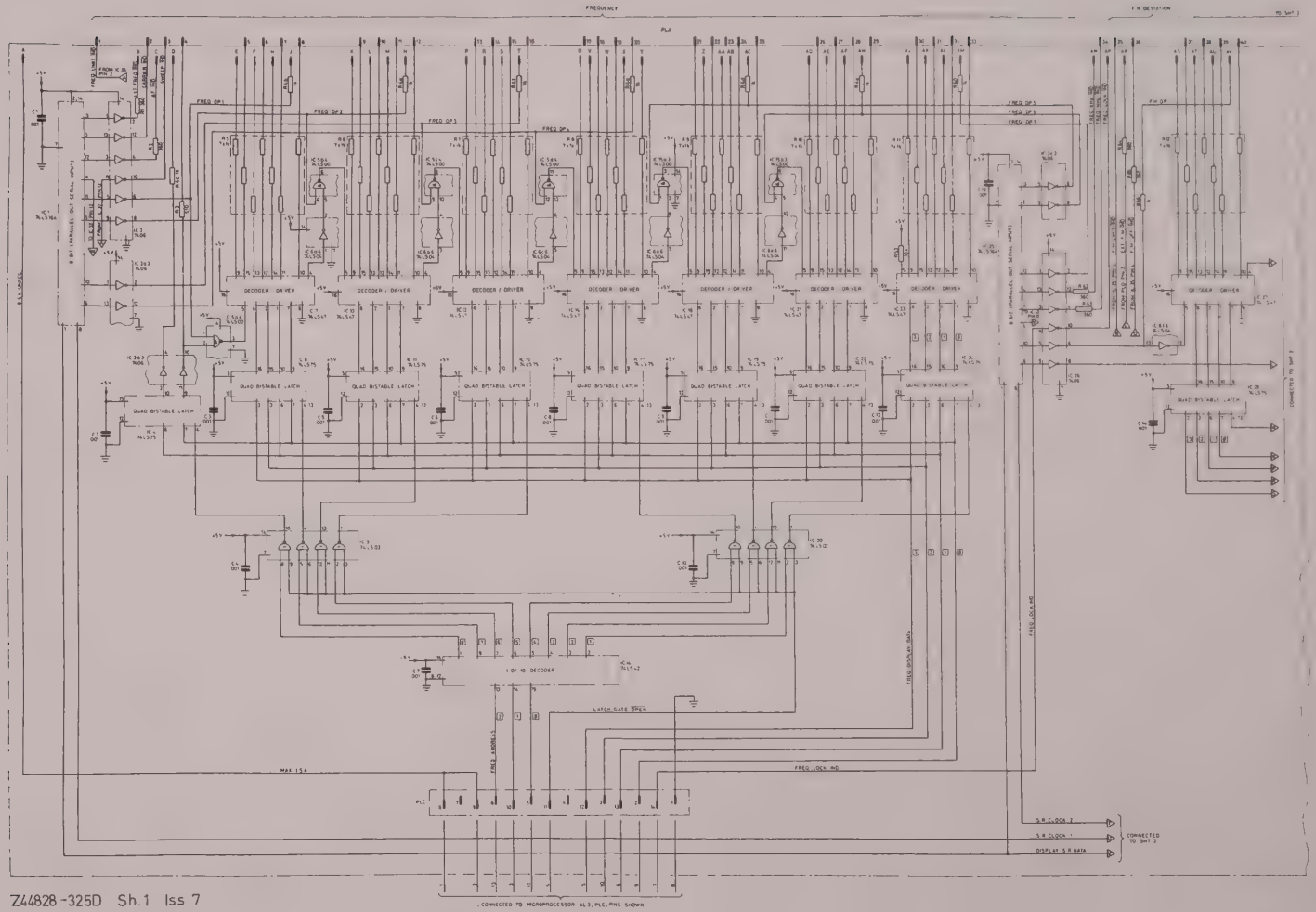
Display, circuit diagram, AL1



Component layout, AL2



Z44828-325D Sh.1 Iss 7

Fig. 8

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Display drive, AL2, circuit diagram, sheet 1

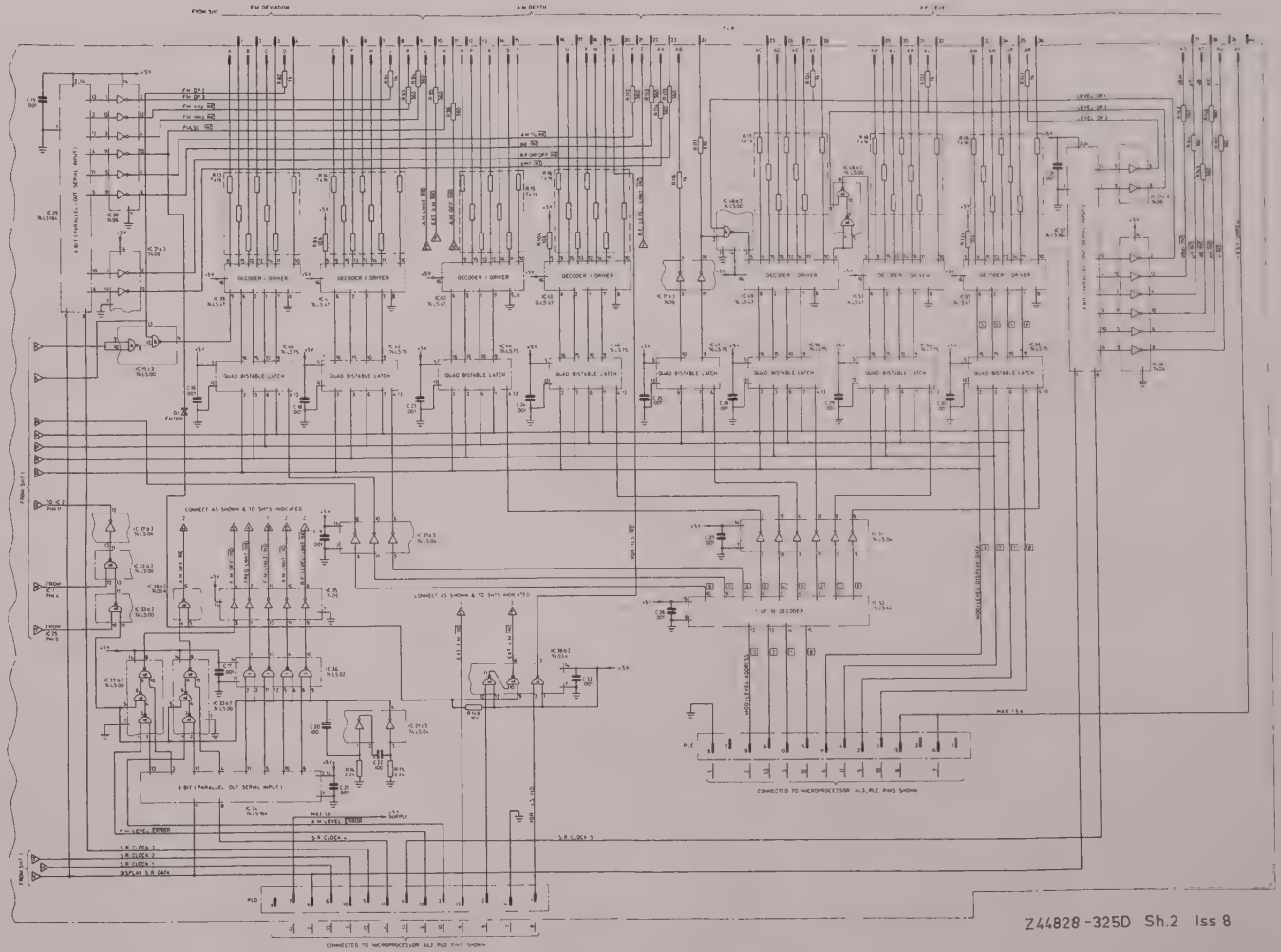

Fig. 9

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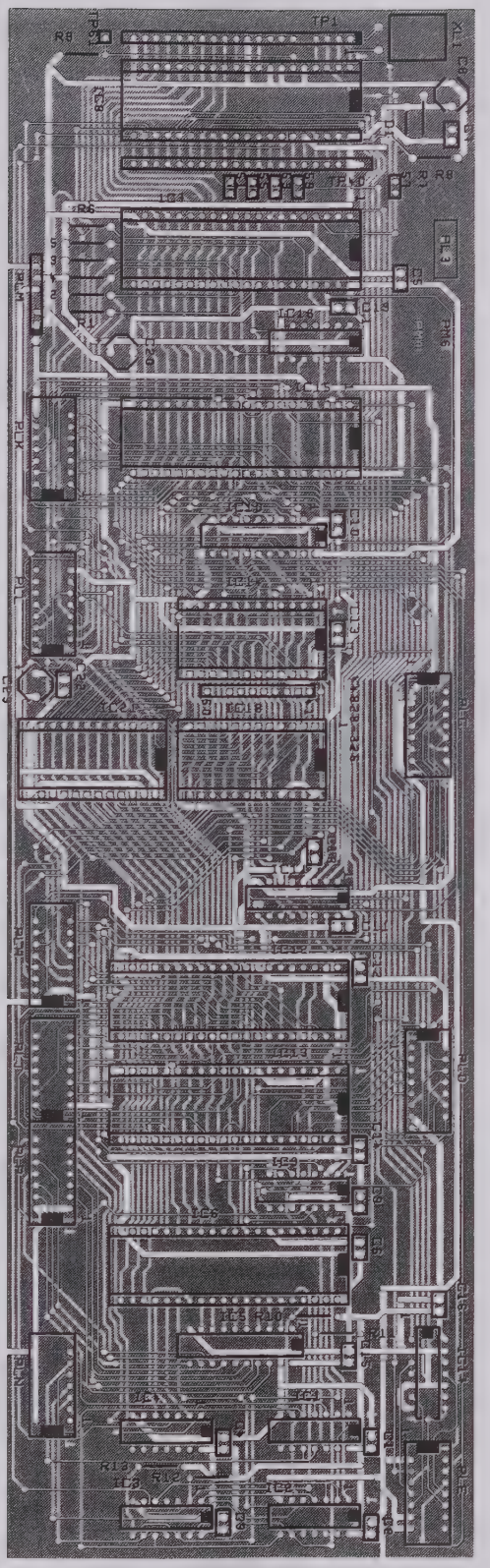
Display drive, AL2, circuit diagram, sheet 2



Component layout, AL3

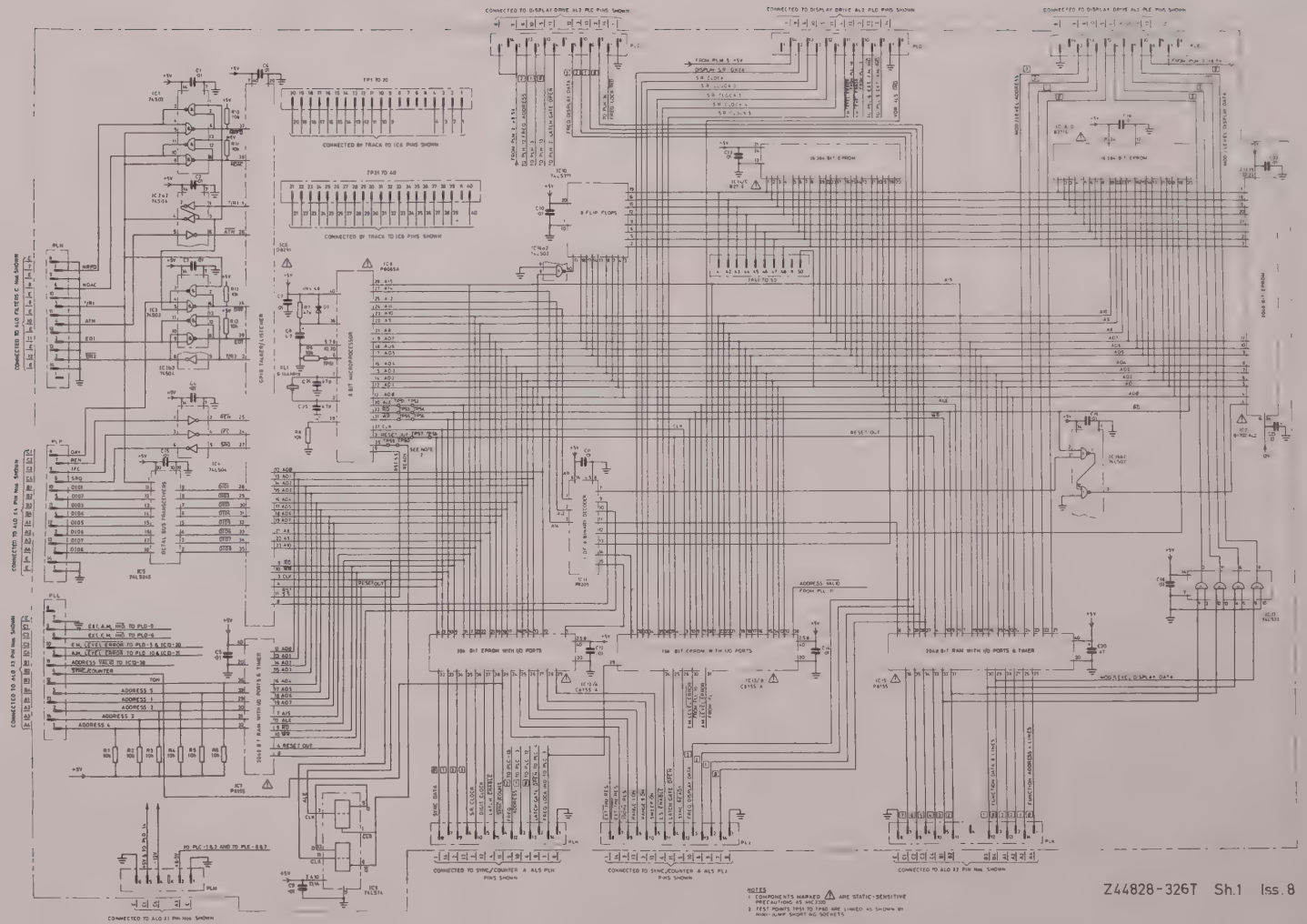


Fig. 10

Microprocessor system, AL3, circuit diagram

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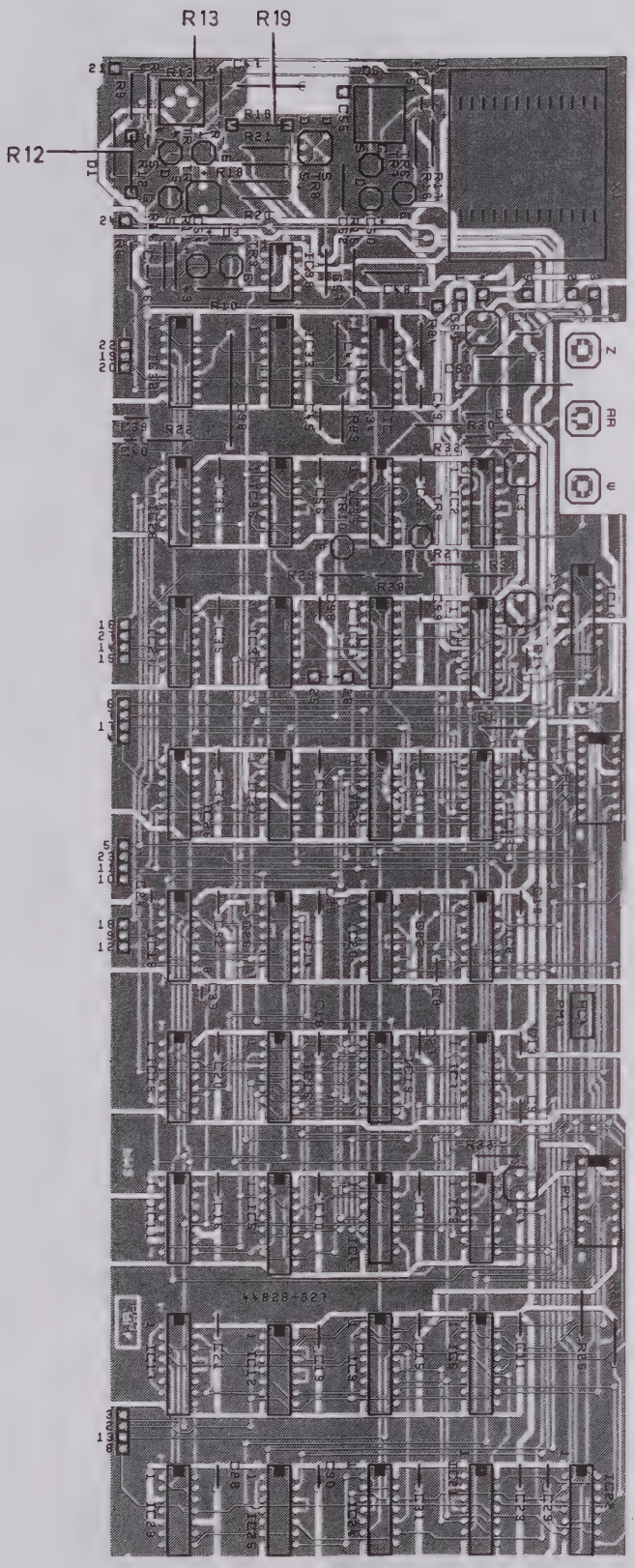
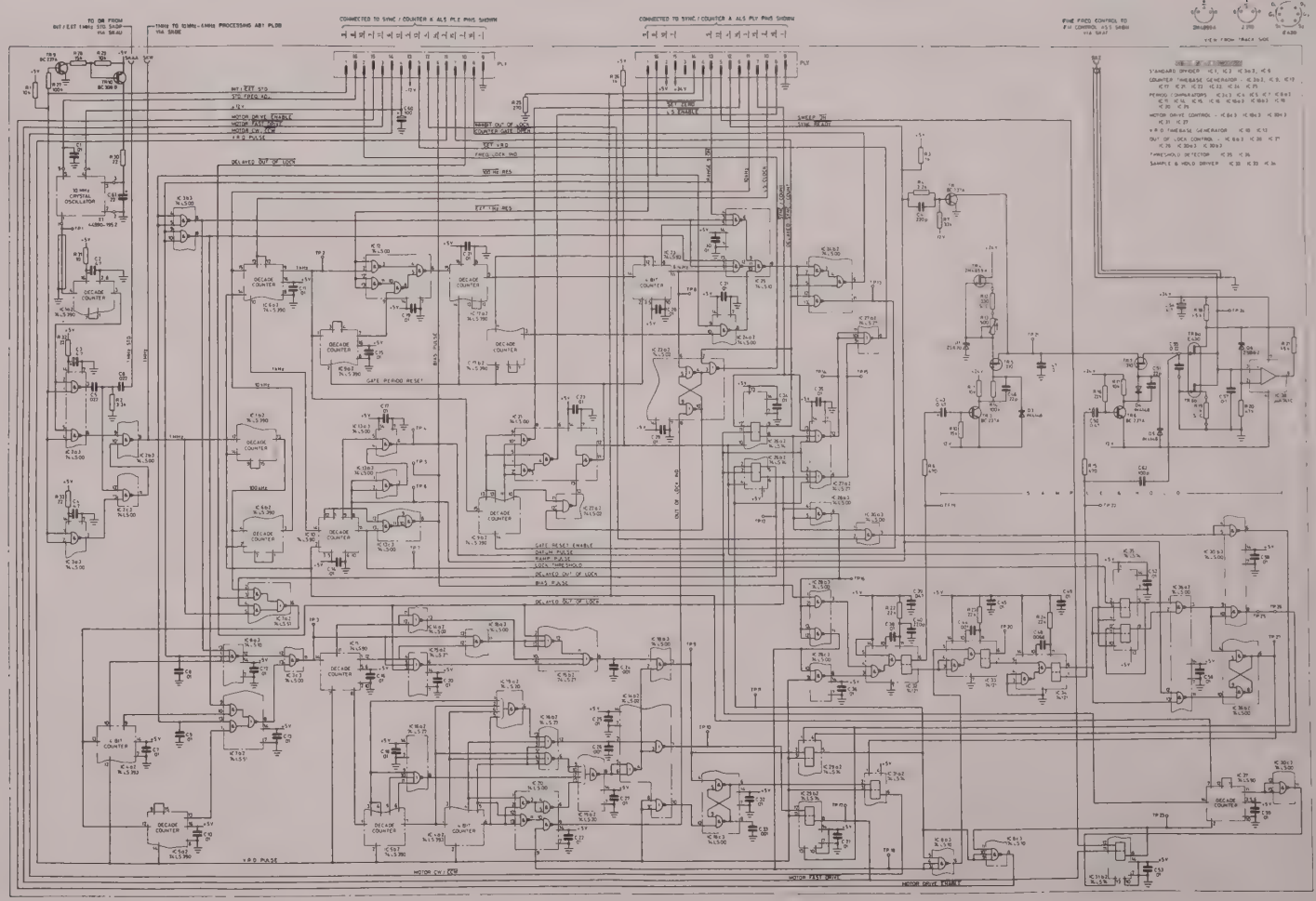


Component layout, AL4



Z44828-327P Sh.1 Iss. 5
Fig. 11

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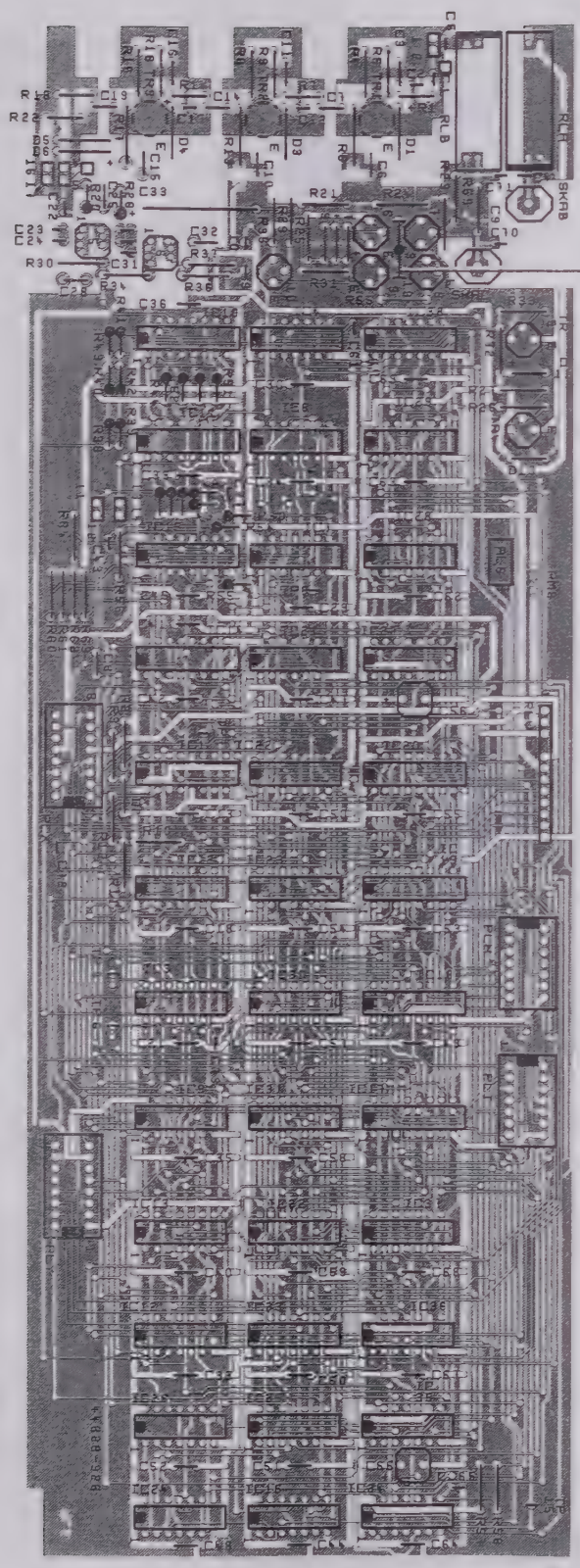
Synchronizer/counter 'B', circuit diagram AL4



Component layout, AL5

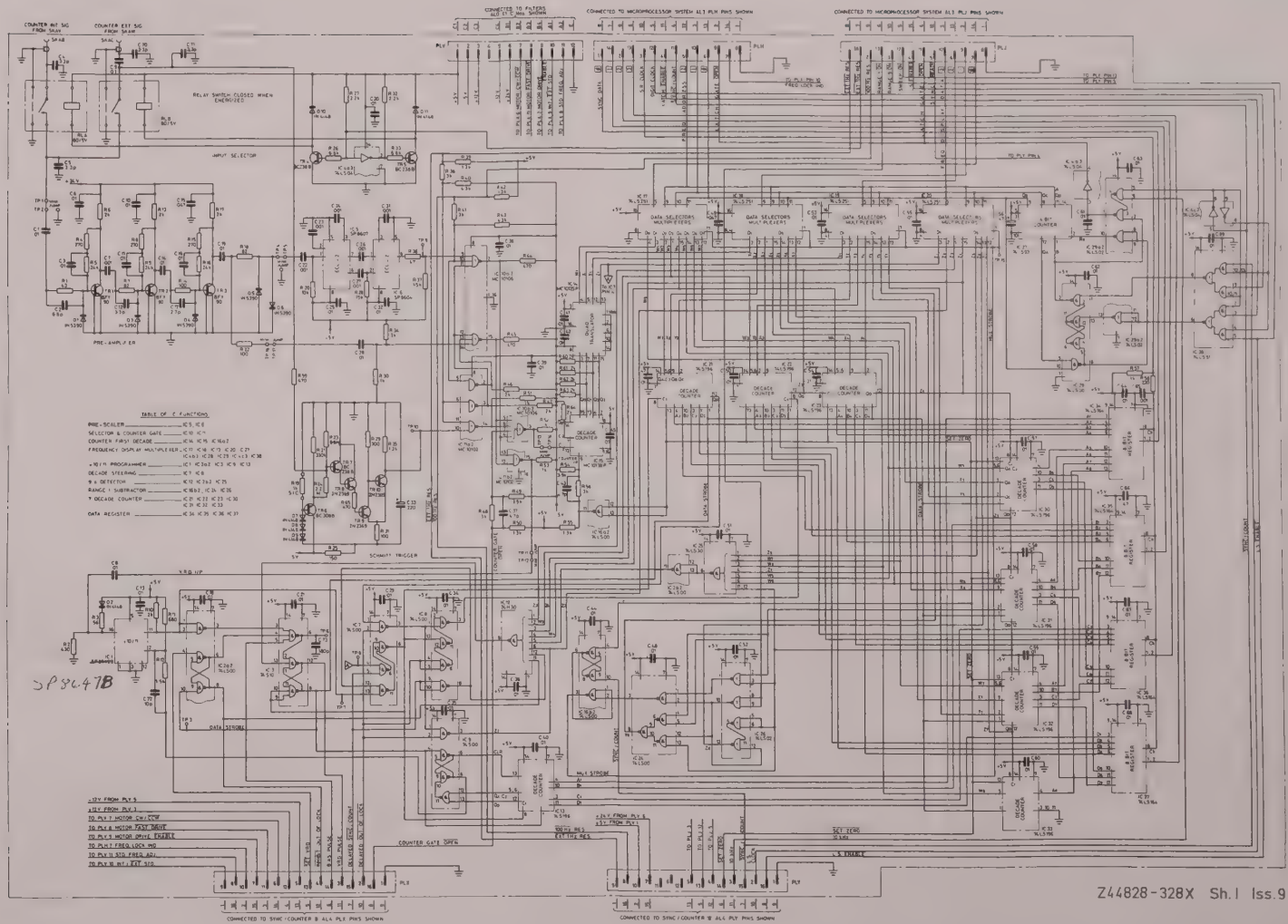


Fig. 12

Synchronizer/counter 'A', circuit diagram AL5

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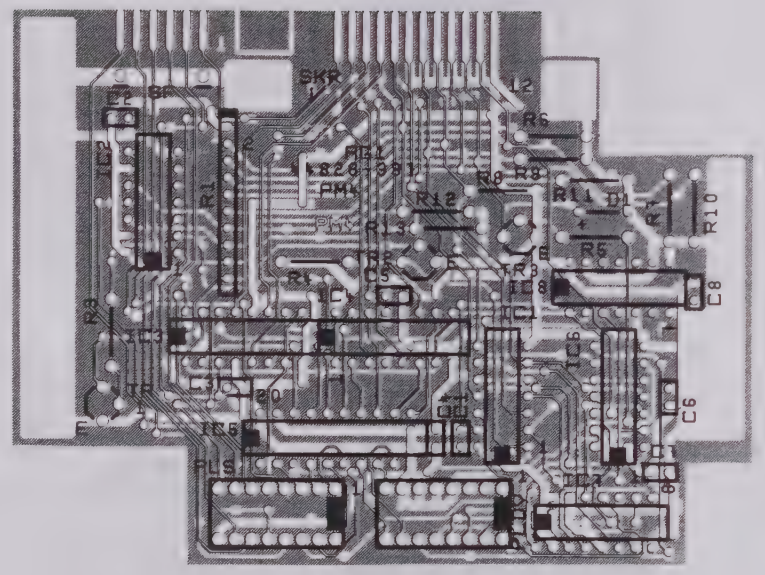

Fig. 13a
Chap. 7
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Component layout, AG1

Fig. 13a

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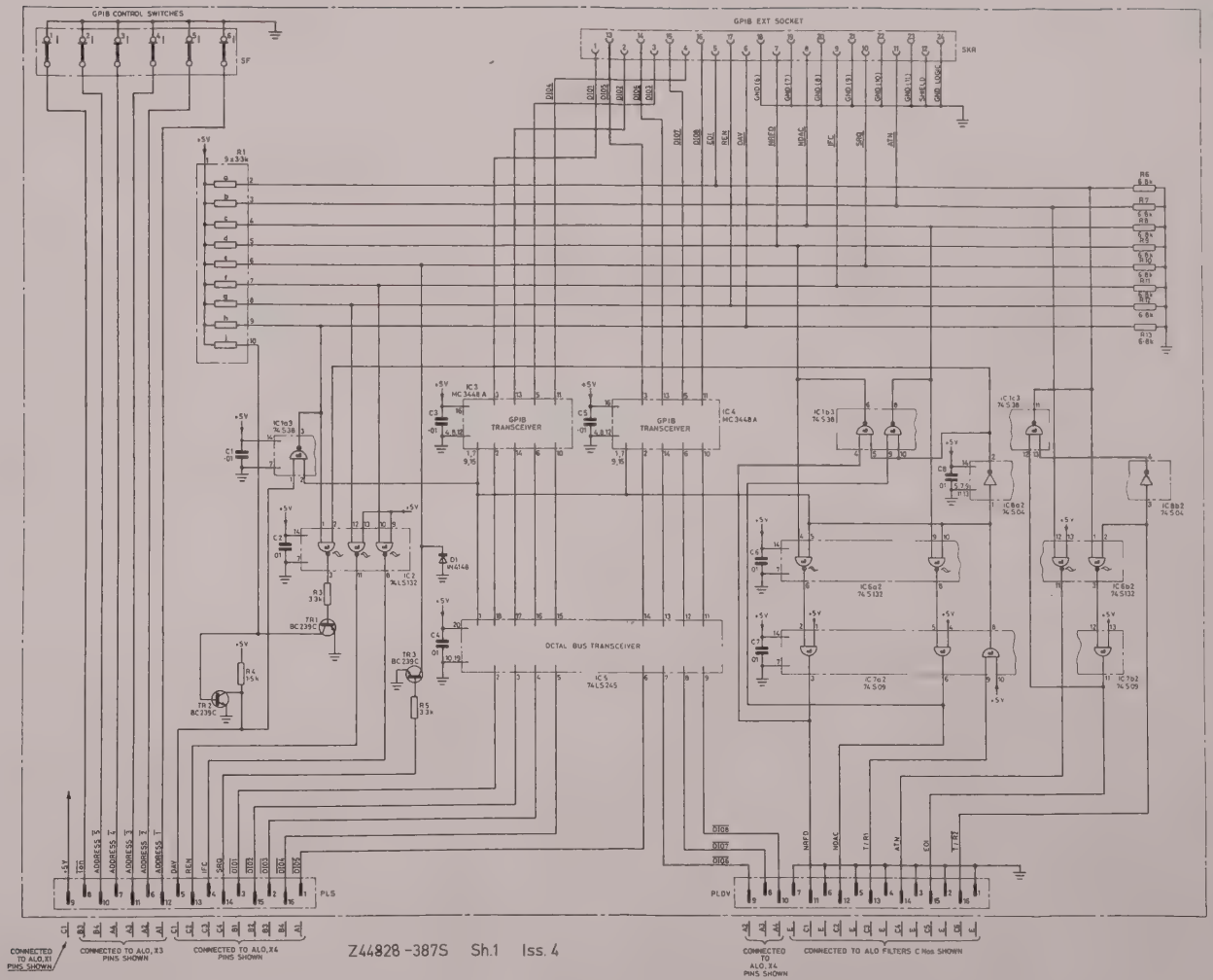

NOTES.
UNDERLINED LABELS REFER TO GPIB TERMS WHICH ARE NEGATIVE TRUE

GPIB ABBREVIATIONS

ATN	ATTENTION
SRQ	SERVICE REQUEST
IFC	INTERFACE CLEAR
DAC	DATA ACCEPTED
NDAC	NOT DATA ACCEPTED
RFD	READY FOR DATA
NRFD	NOT READY FOR DATA
DAV	DATA VALID
EOI	END OR IDENTIFY
DIO	DATA INPUT/OUTPUT
REN	REMOTE ENABLE
ton	TALK ONLY

Fig. 13
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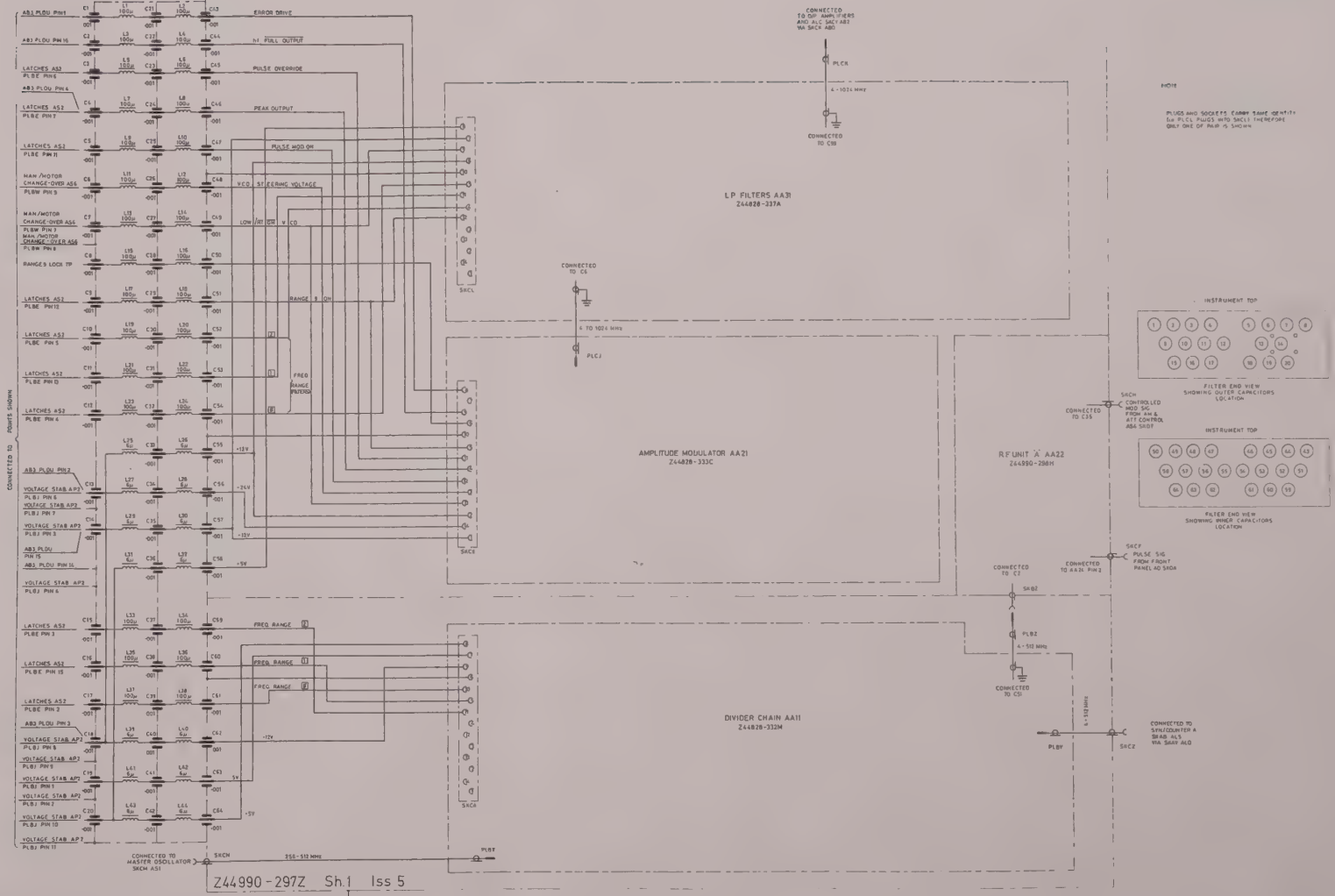
GPIB drive, AG1, circuit diagram



RF section 'A', interconnections AA0

Fig. 14

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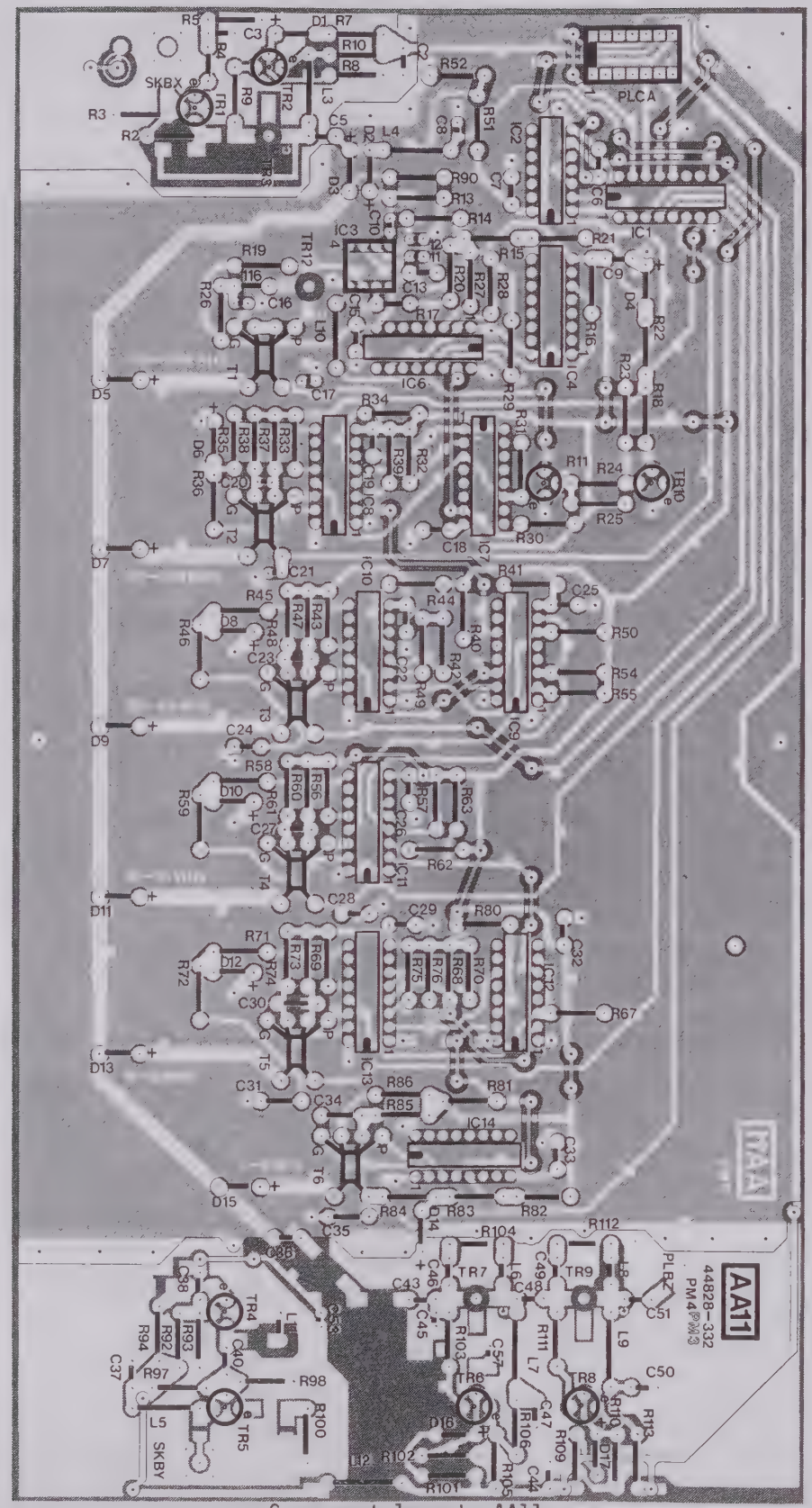

Component layout, AA11

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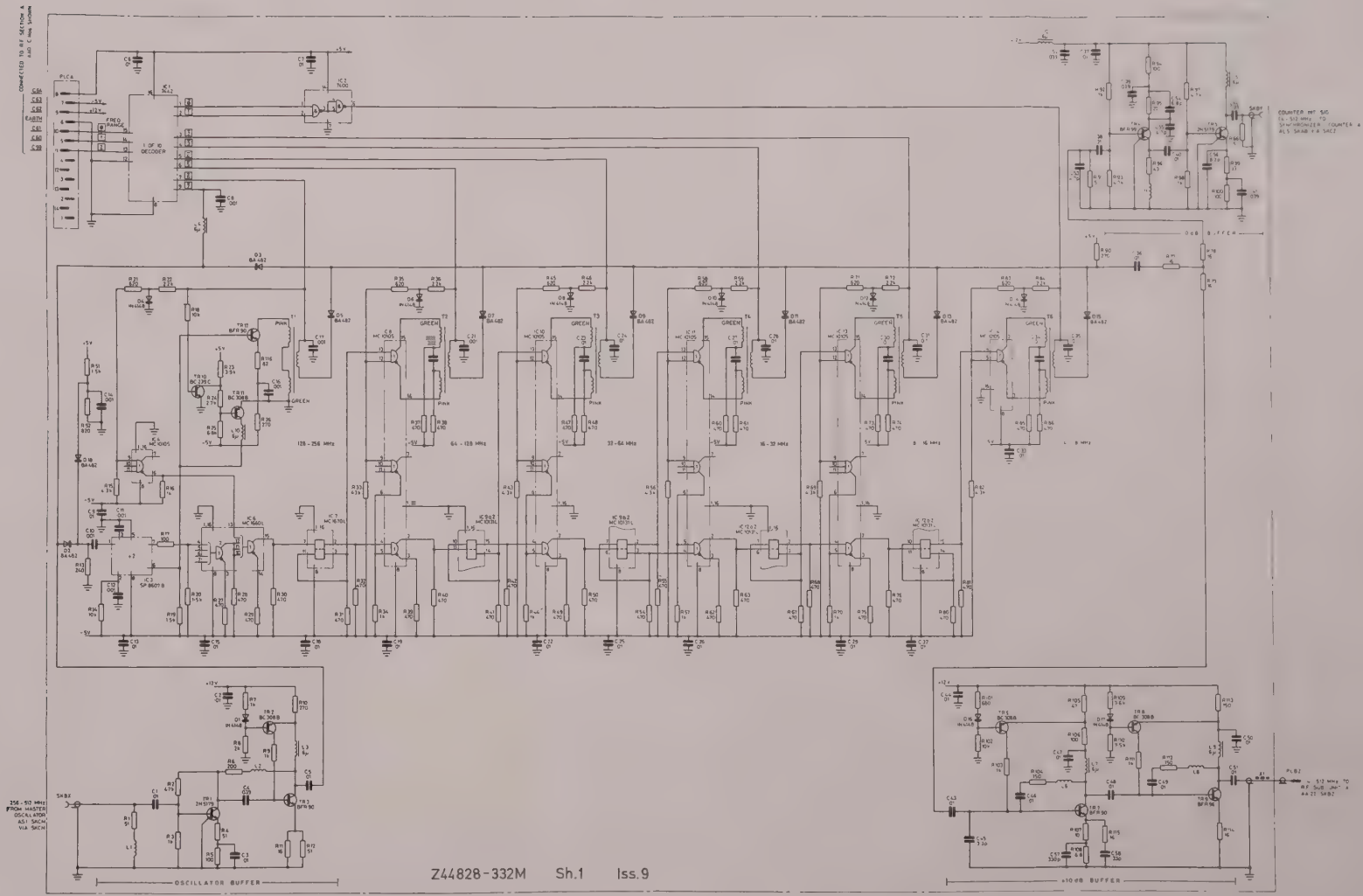

Fig. 15

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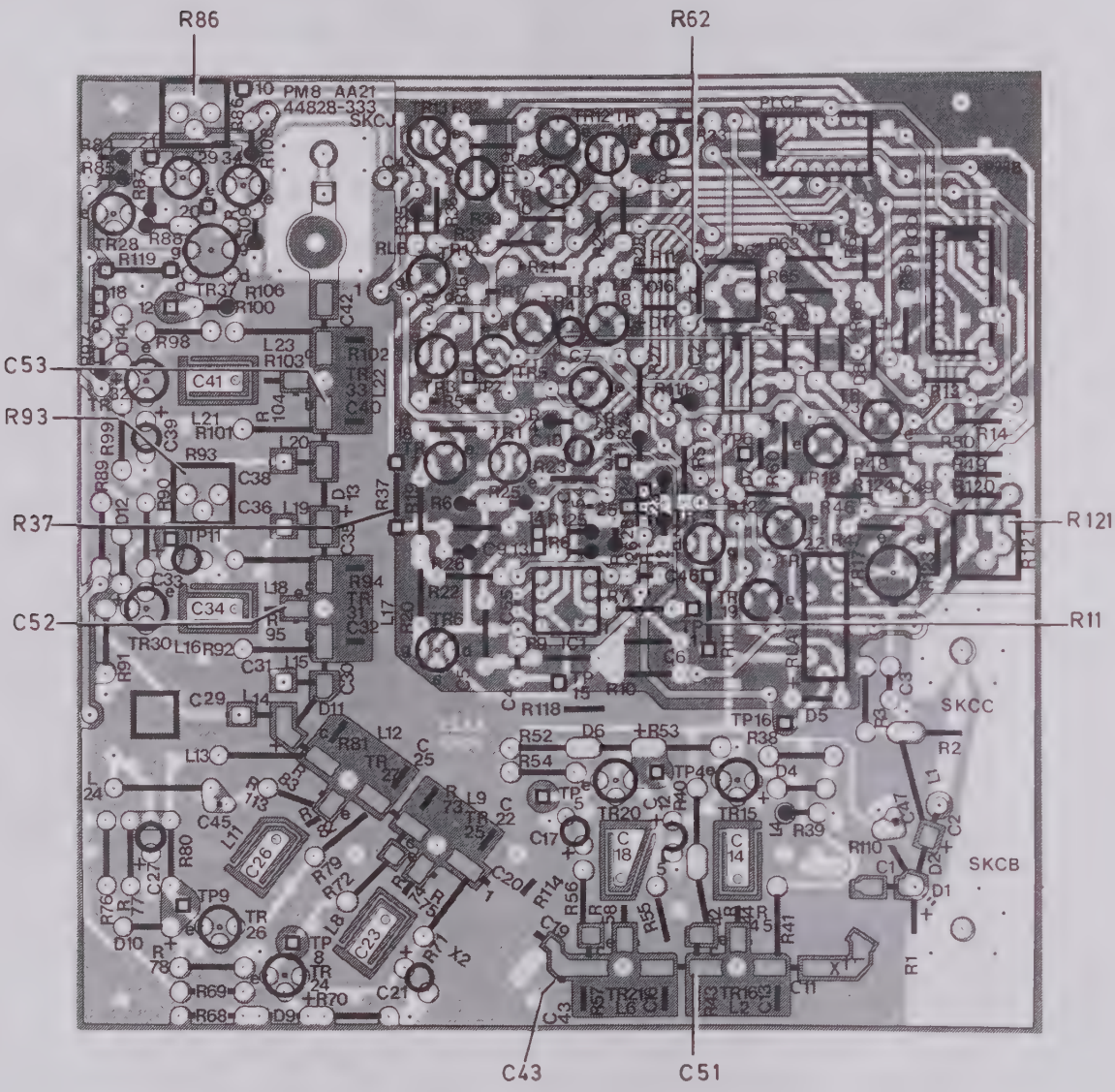
Divider chain, AA11, circuit diagram



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Component layout, AA21

Fig. 16a

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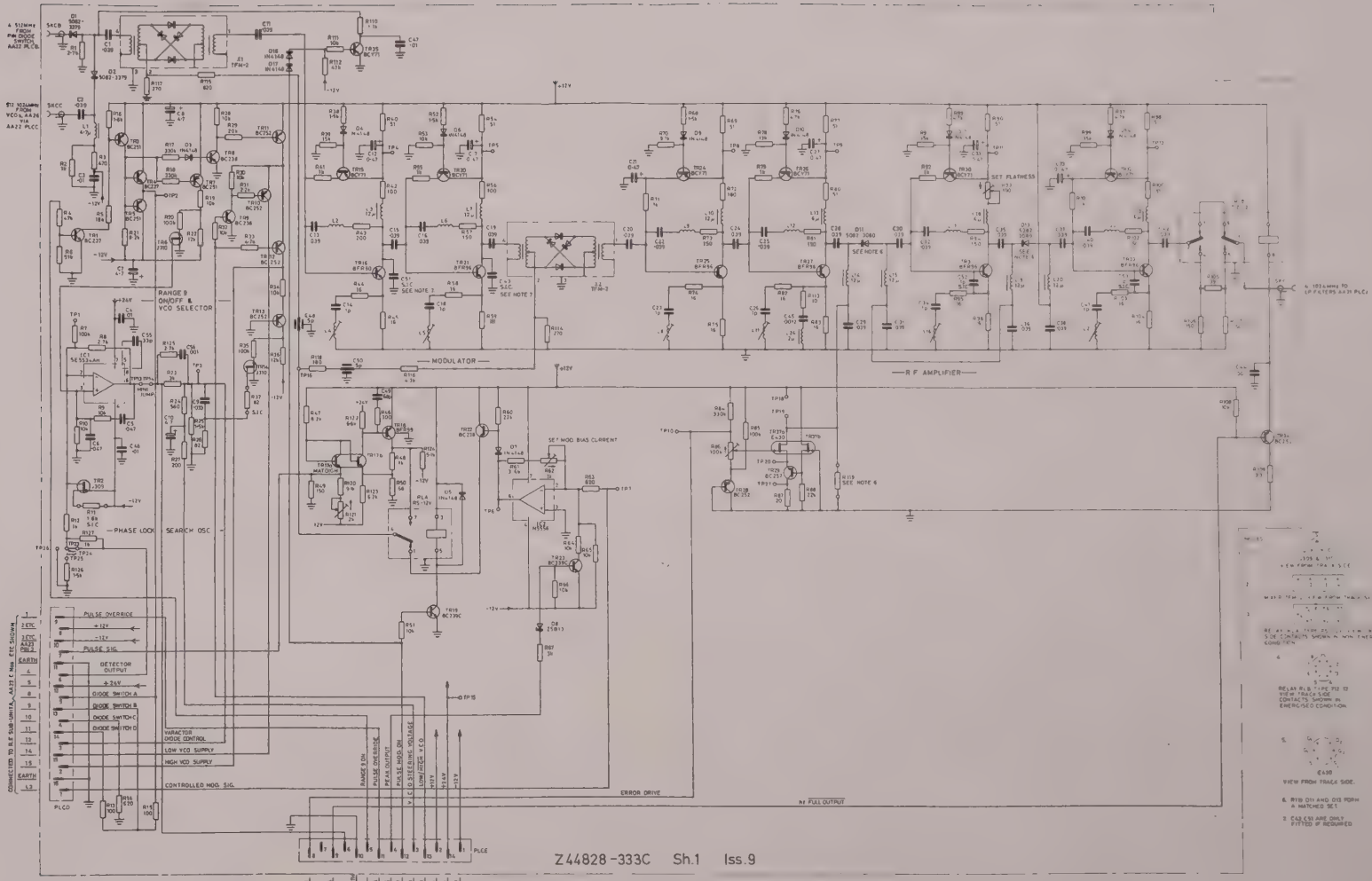

Fig. 16

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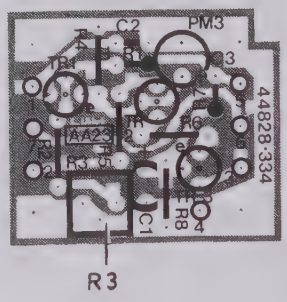
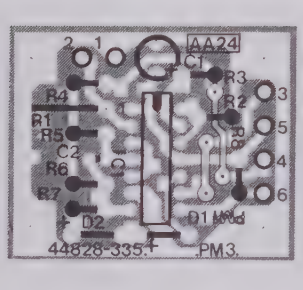
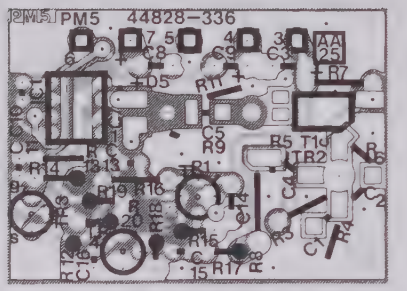
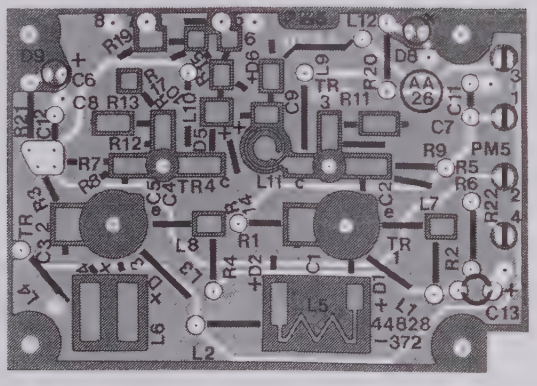
Amplitude modulator, AA21, circuit diagram









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Component layout, AA22

Fig. 17a

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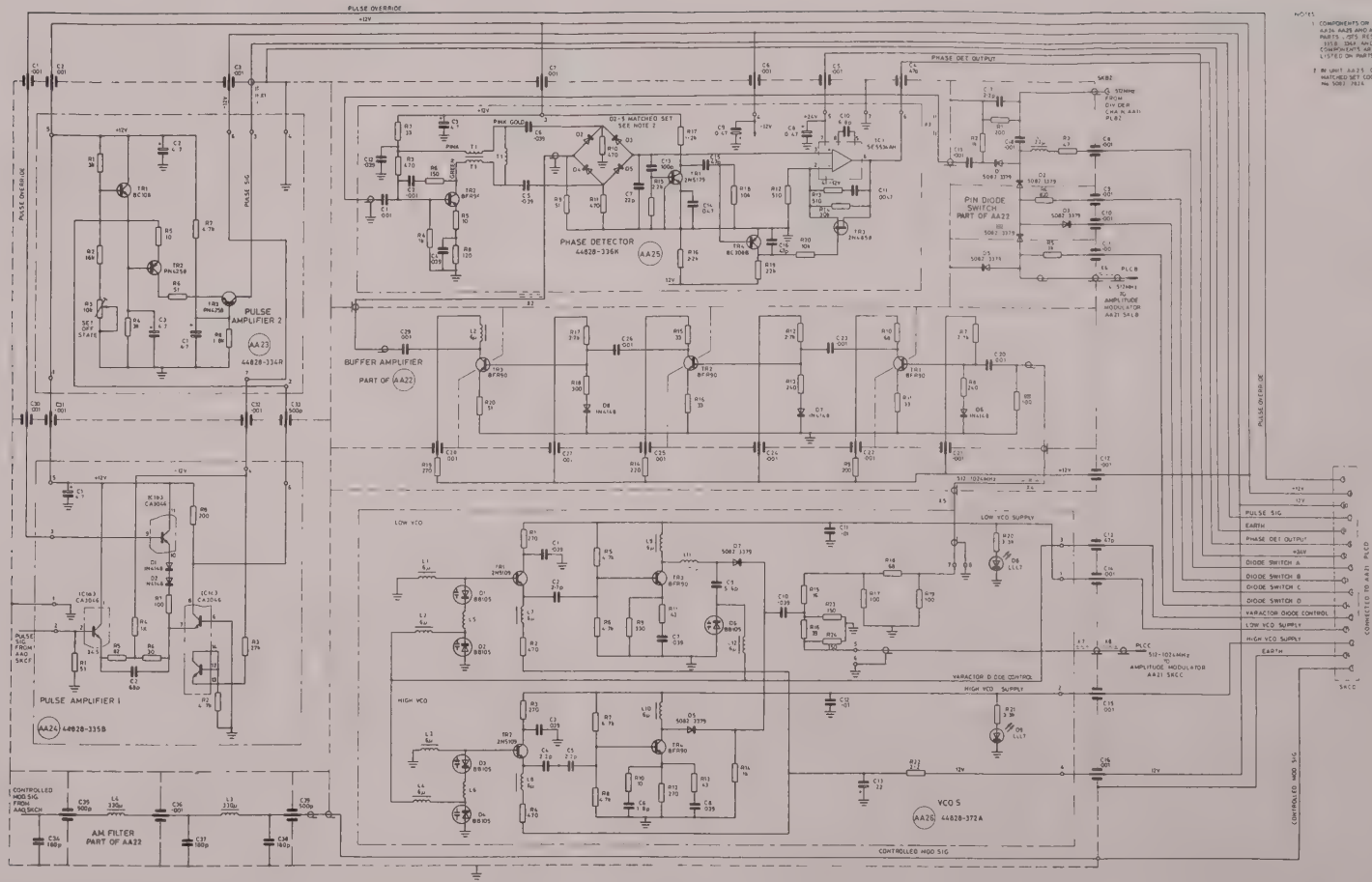

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Fig. 17

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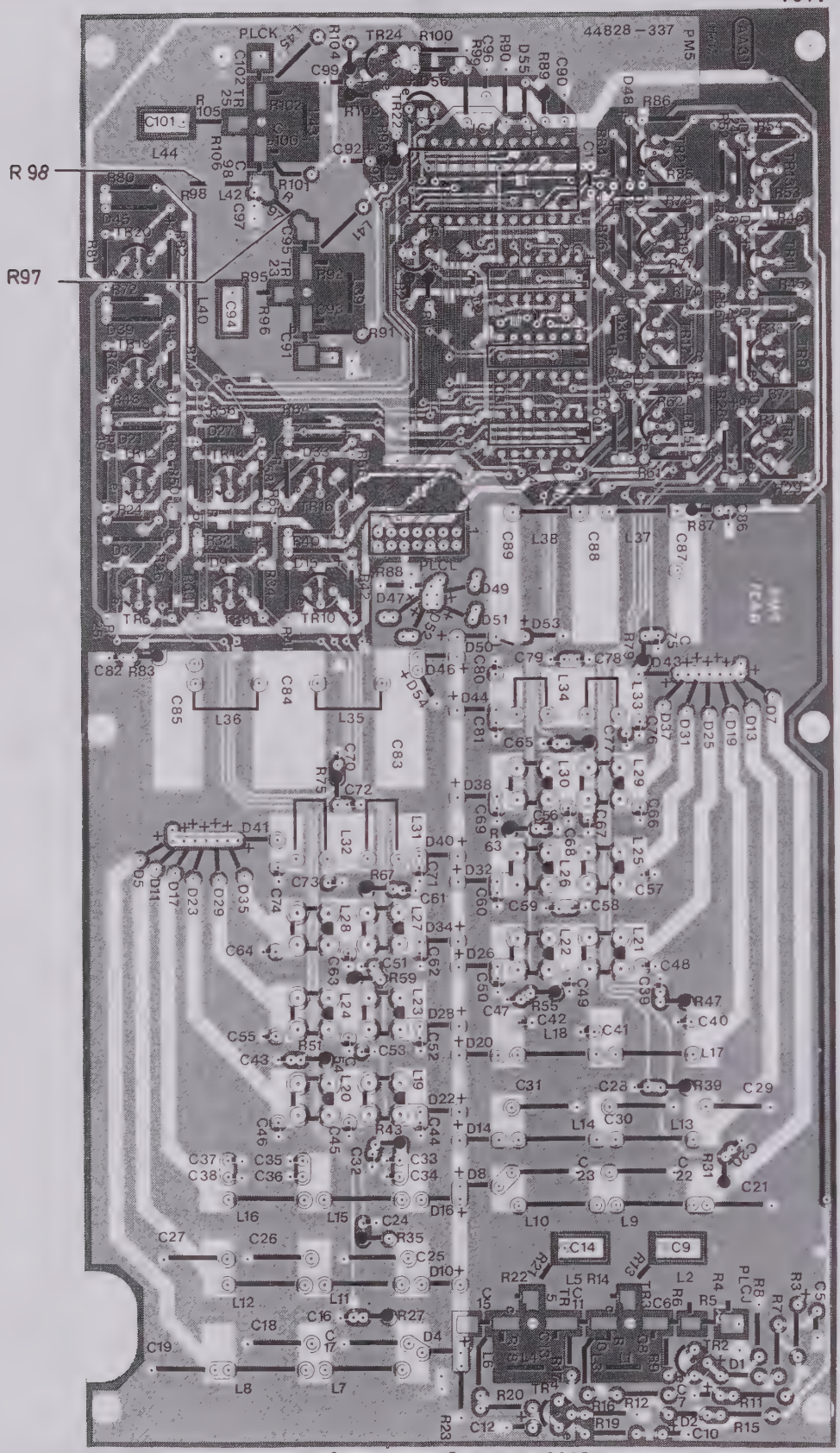
RF sub-unit 'A', AA22, circuit diagram
comprising boards AA23, AA24, AA25 and AA26



Component layout, AA31

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Fig. 18a

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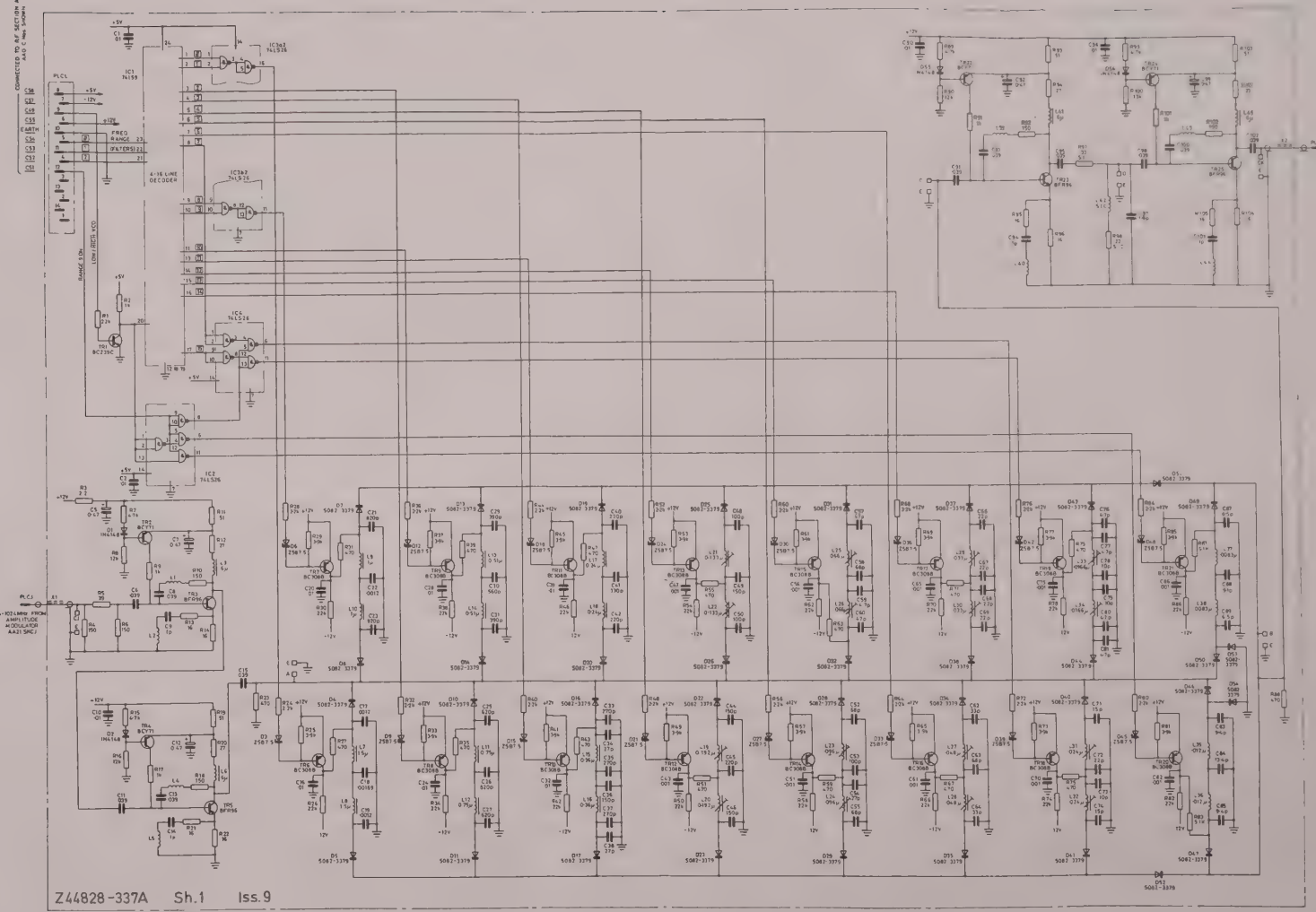

Fig. 18

LP filters, AA31, circuit diagram

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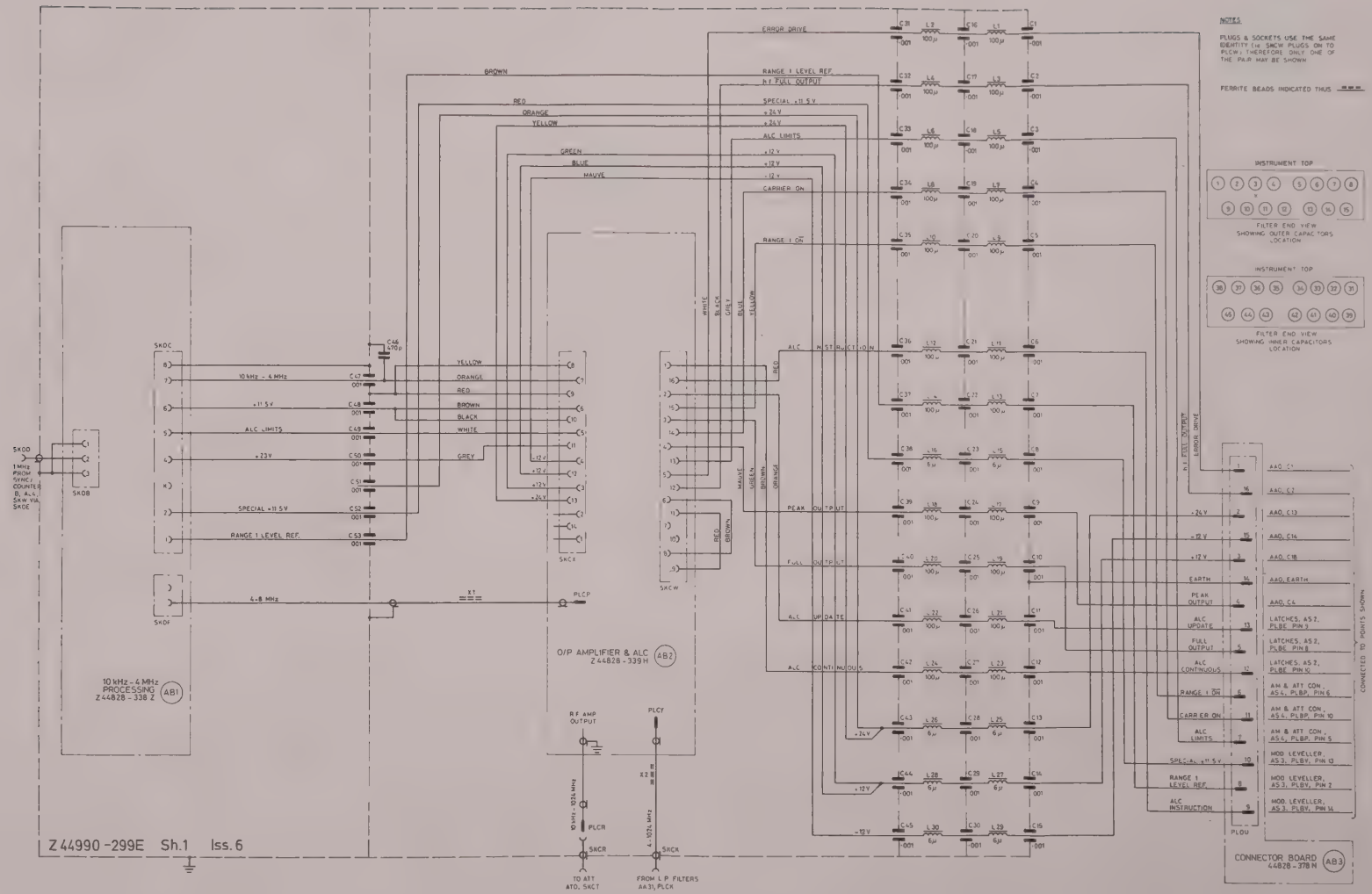

Fig. 19

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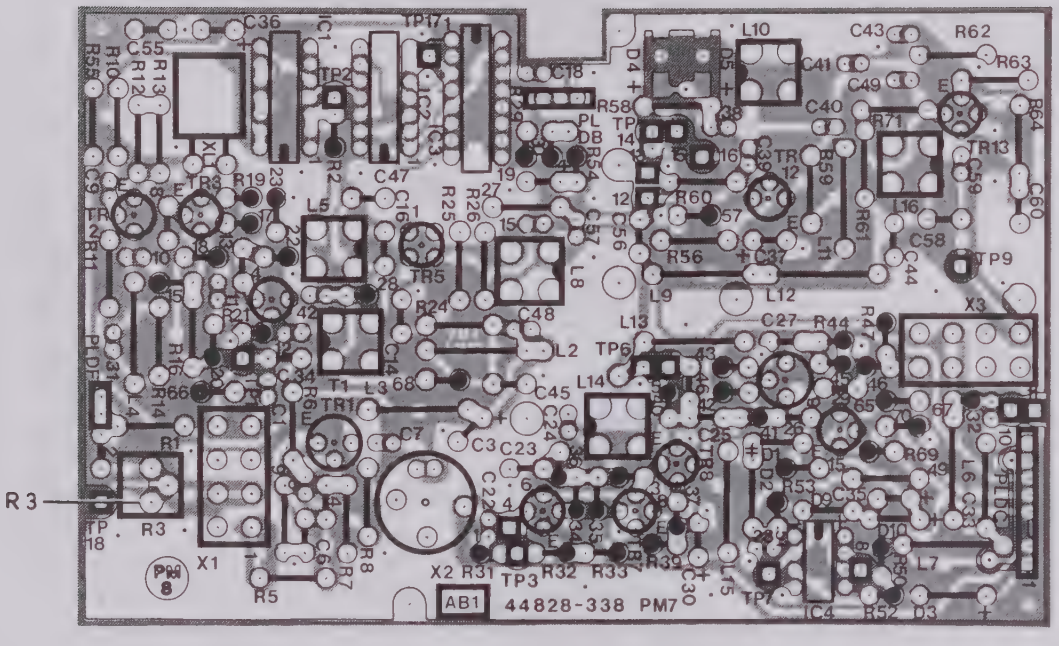
RF section 'B', interconnections, ABO



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Component layout, AB1

Fig. 20a

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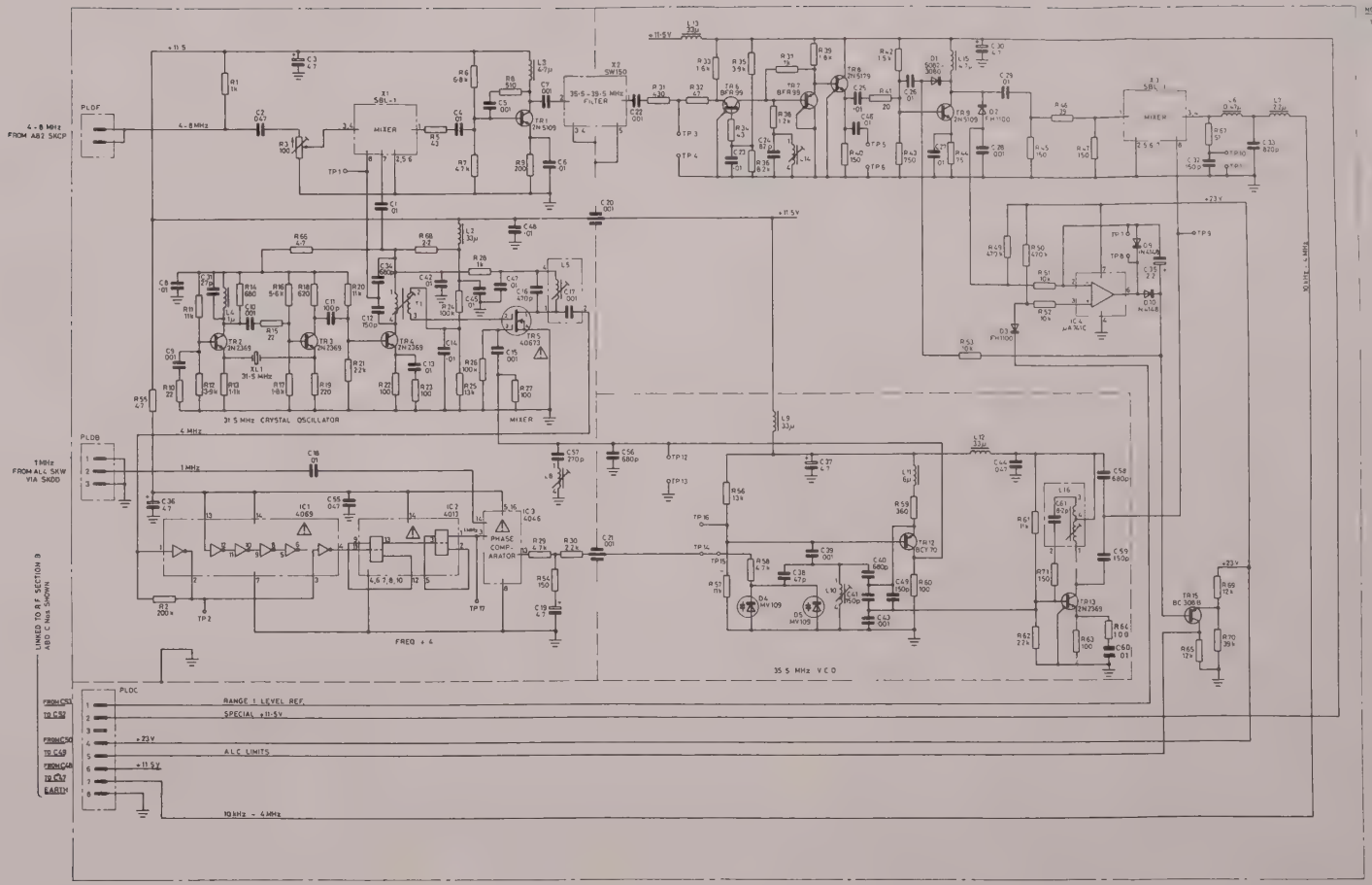

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Fig. 20

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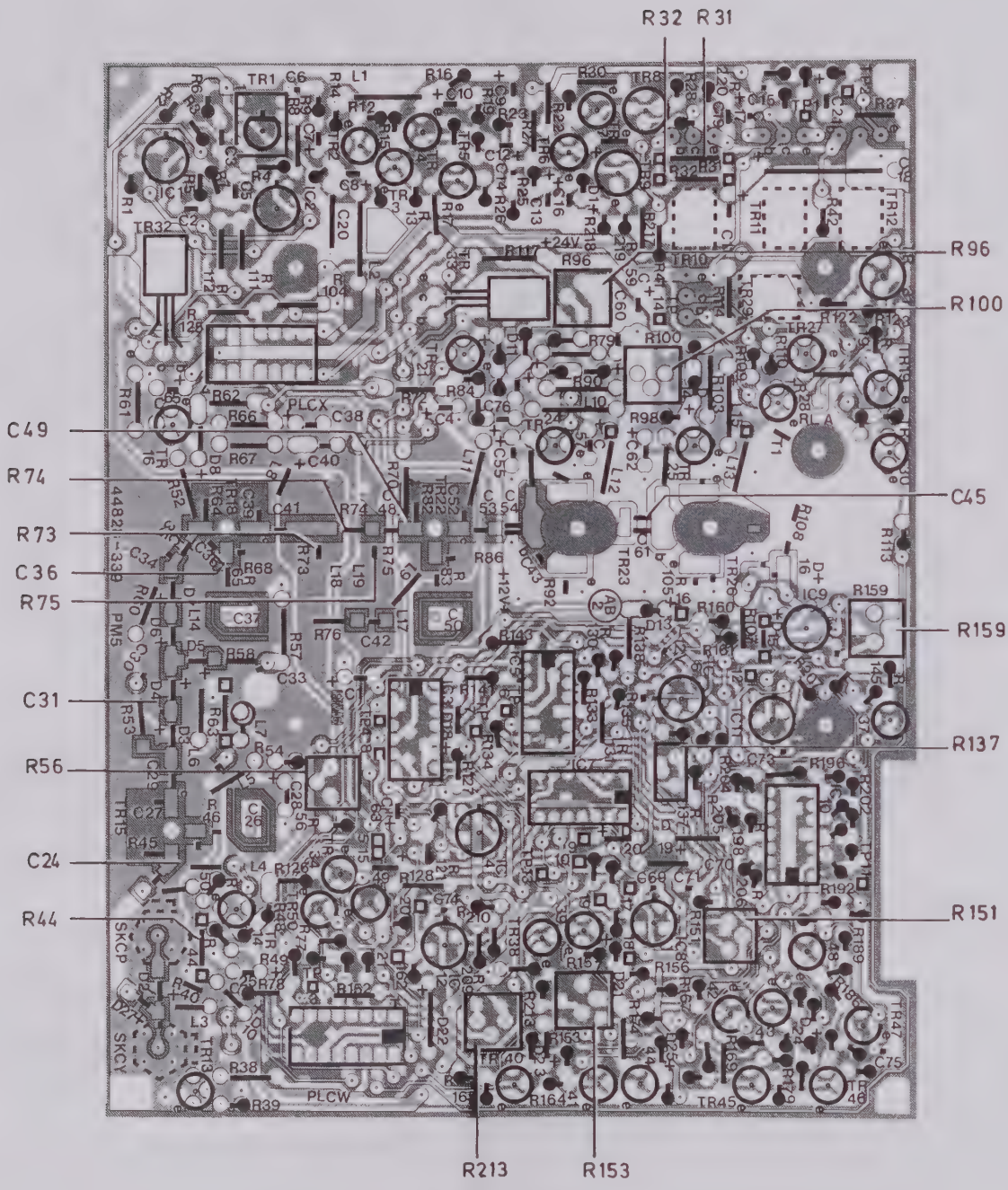
10 kHz-4 MHz processing, AB1, circuit diagram



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Component layout, AB2

Fig. 21a

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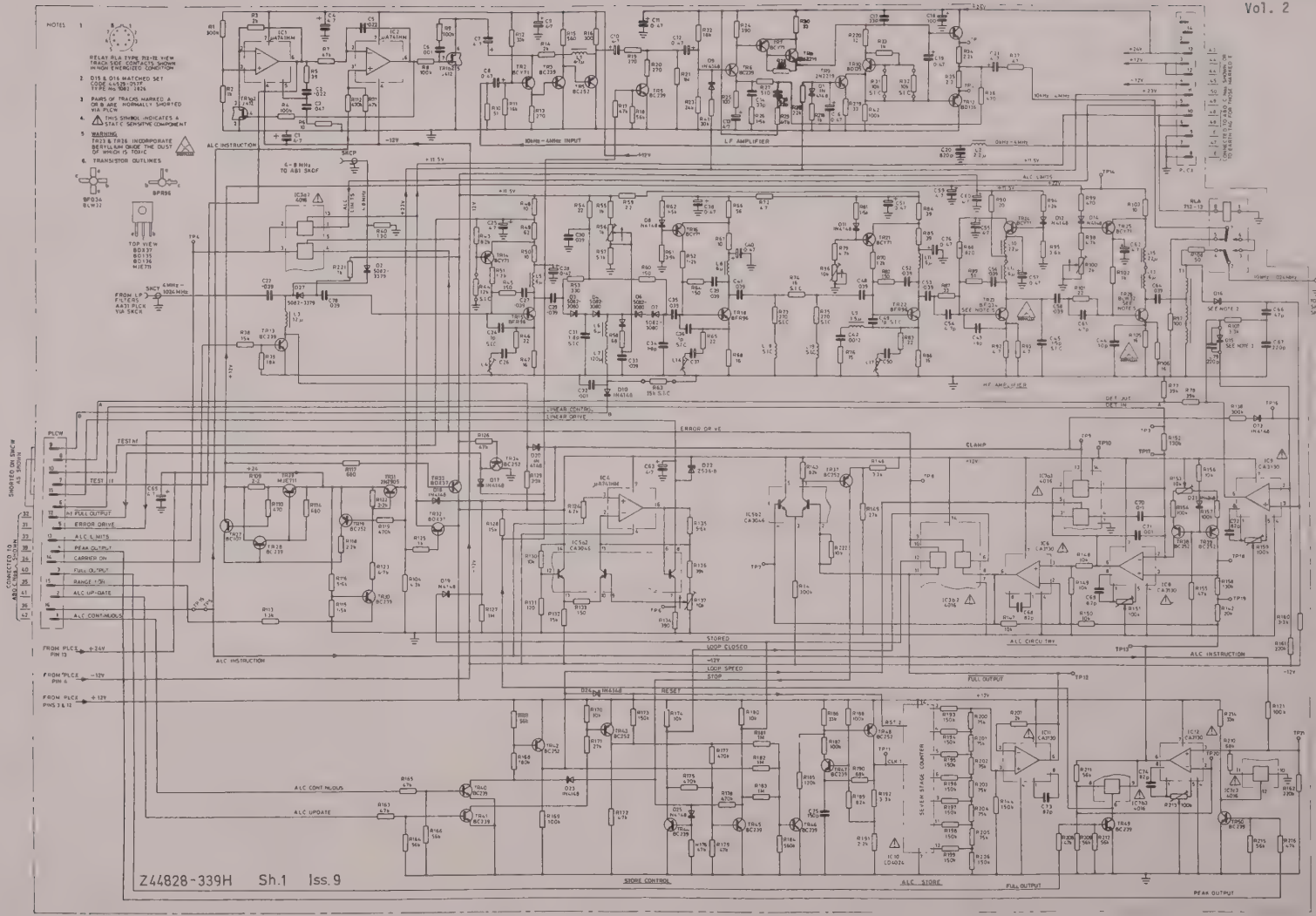

Fig. 21

Output amplifiers and ALC, AB2, circuit diagram

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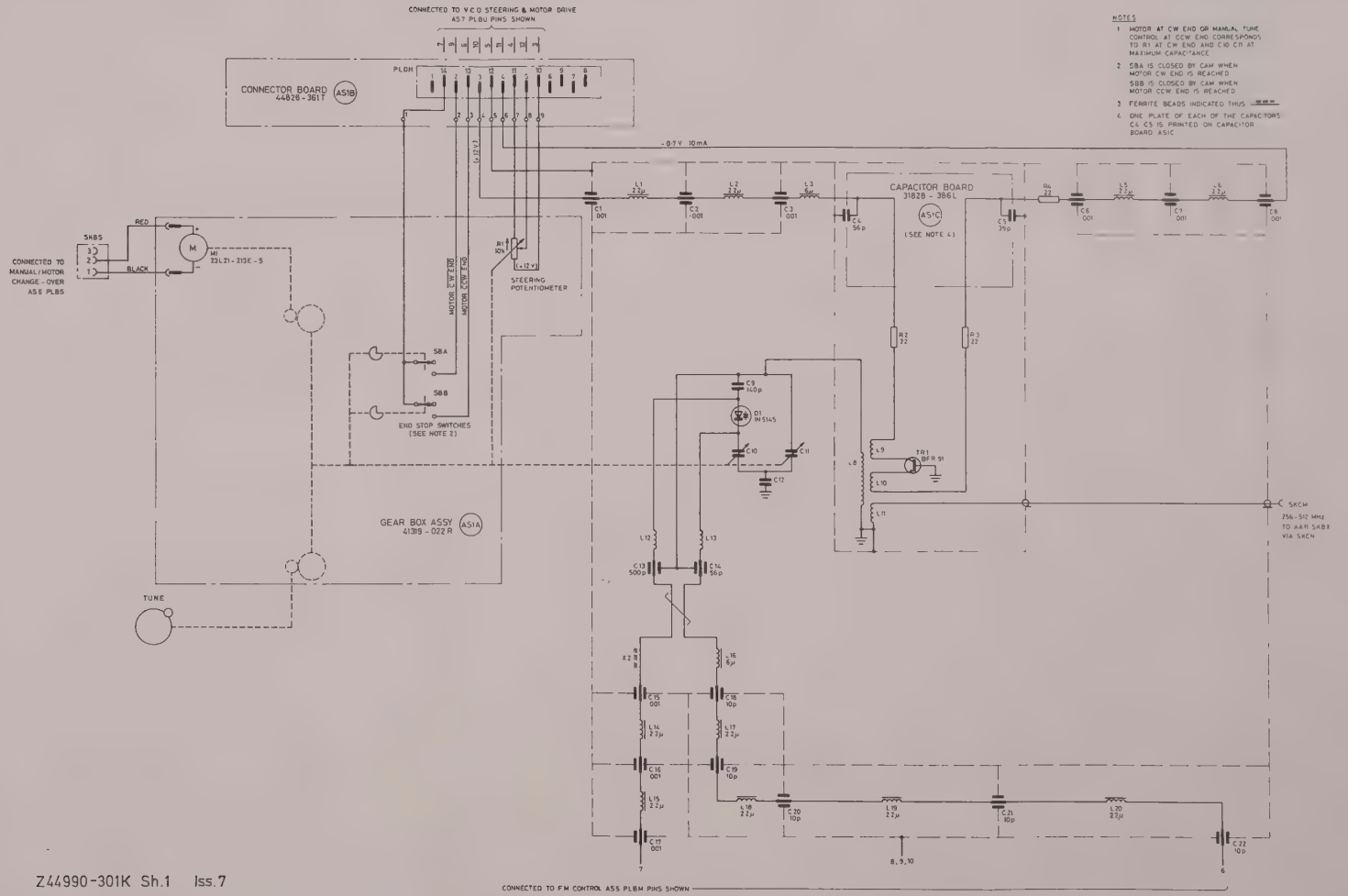
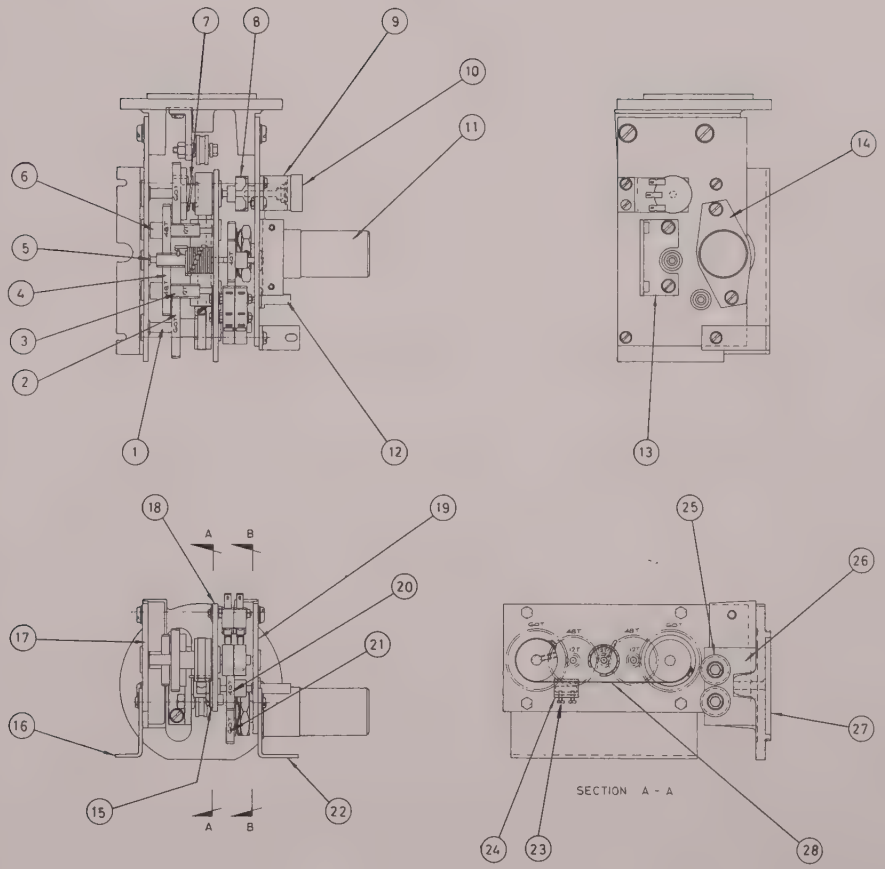


Z44990-301K Sh.1 Iss.7

Fig. 22

Apr. 81

Master oscillator, AS1, circuit diagram



E41319-022R Sh.1 Iss.3

Item No.	Item	Code No.
1	Cam shaft	33900-608N
2	Spur gear 60T	31319-013U
3	Spur gear 12T	31319-016L
4	Spur gear 48T	31319-014Y
5	Shaft	33900-609L
6	Shaft	33900-610Y
7	Spring	31119-041F
8	Flexible coupling	22713-219J
9	Bracket	35902-465C
10	Variable resistor R1 10kΩ 5% 2W	25725-406F
11	Motor gearbox	23535-498C
12	Drive shaft	33900-588M
13	Bracket	35902-805T
14	Motor plate	35902-073F
15	Support	35903-221Z
16	Angle	35902-540B
17	Bearing plate	35902-130K
18	Bearing plate	35902-129Z
	Ball bearings for item 17 & 18 (8 off)	22631-298T
	Ball bearings for item 17 & 17 (4 off)	22631-299P
19	Bearing plate	35903-216K
20	Spur gear 40T	31319-015N
21	Spur gear 60T	31319-017J
22	Bracket	35902-541K
23	Screw, polycarbonate	21836-003X
24	Clamp	37490-527G
25	Cam nut	33900-911A
26	Support angle	34900-713U
27	Support casting	35890-059N
28	Spring	31119-044S
29	Micro-switch (SBA,SBB)	23483-124C

Fig. 23

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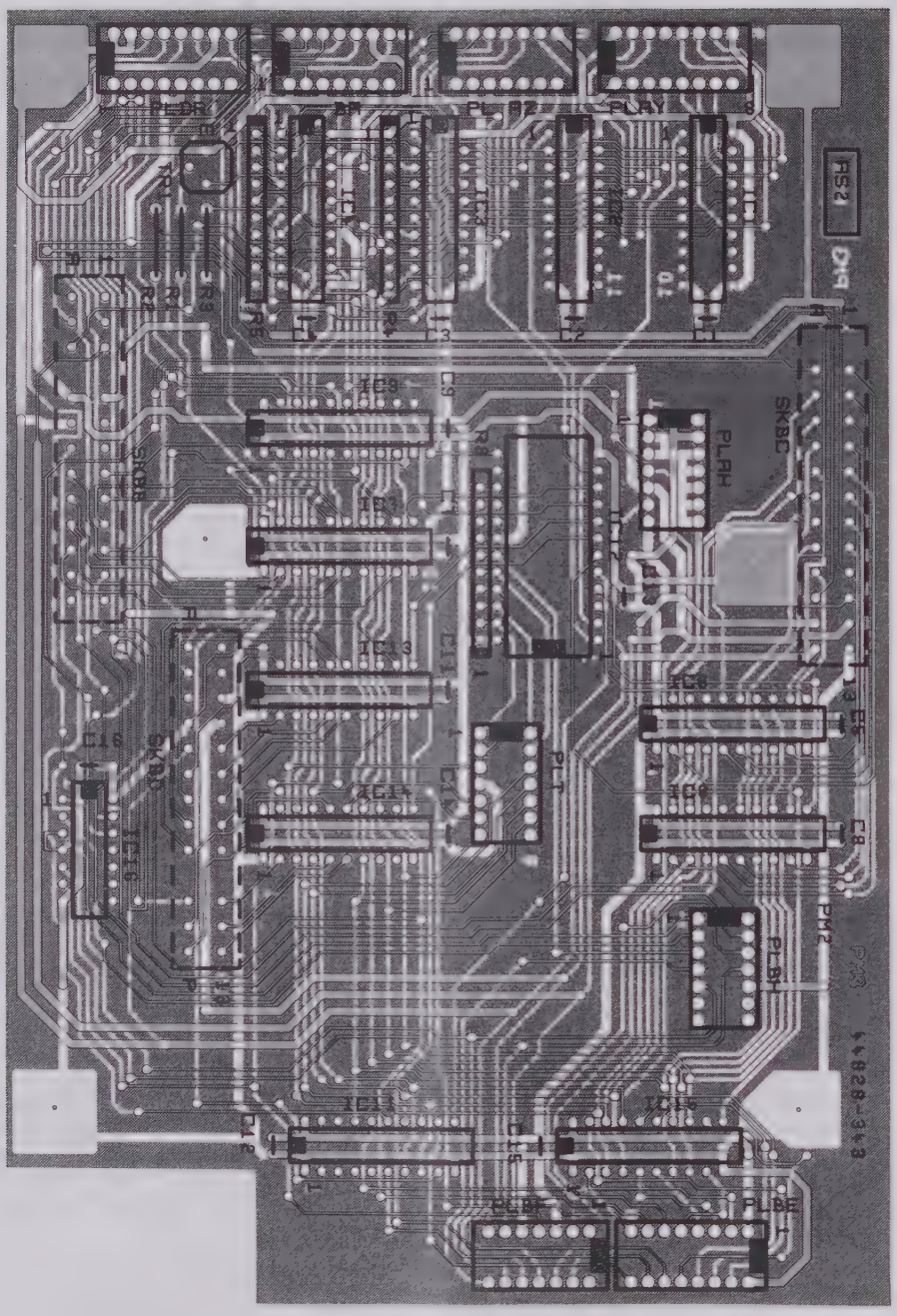
Master oscillator gearbox, AS1, assembly diagram



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Component layout, AS2

Fig. 24a

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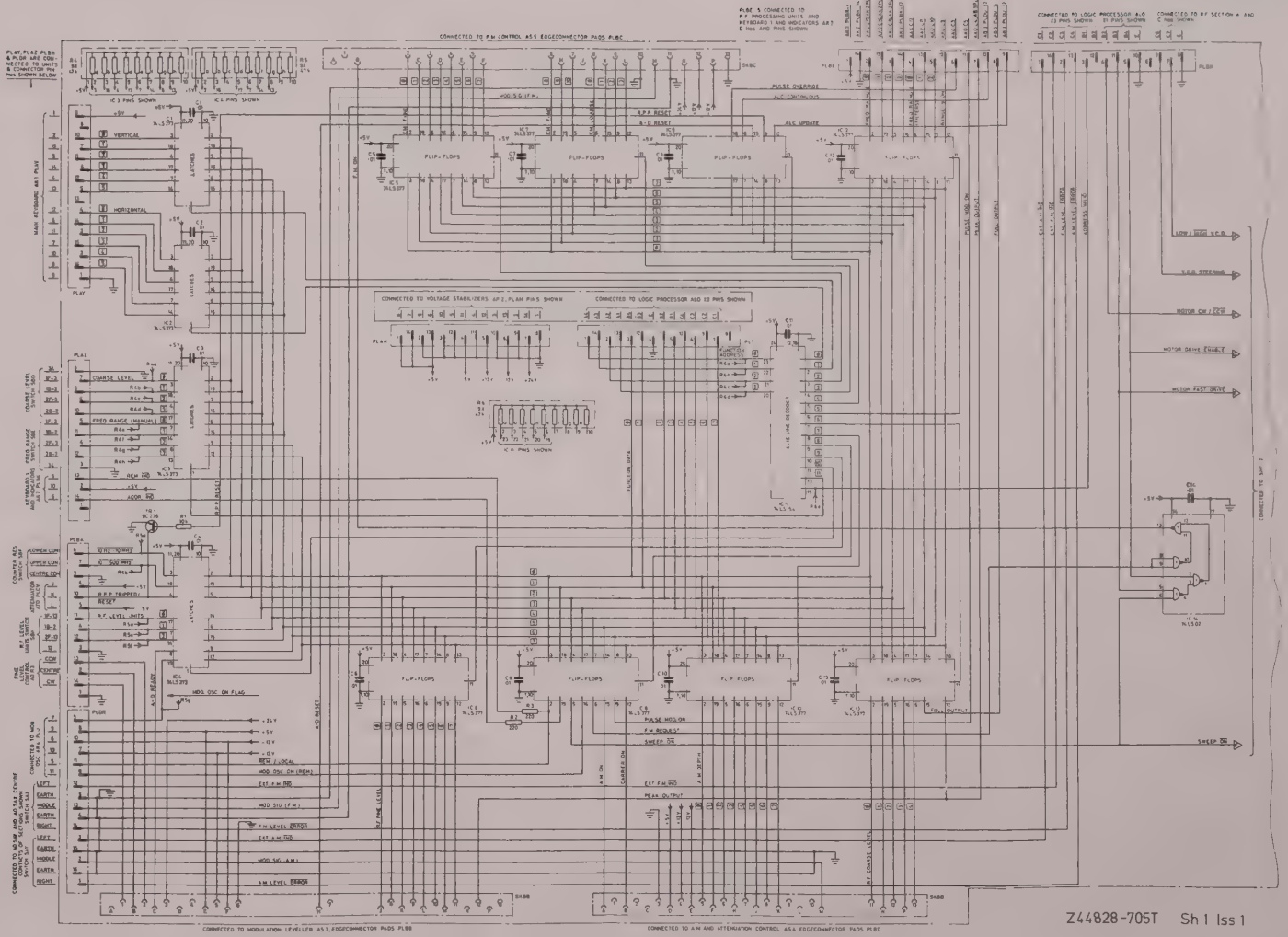

Fig. 24

Latches, AS2, circuit diagram, sheet 1

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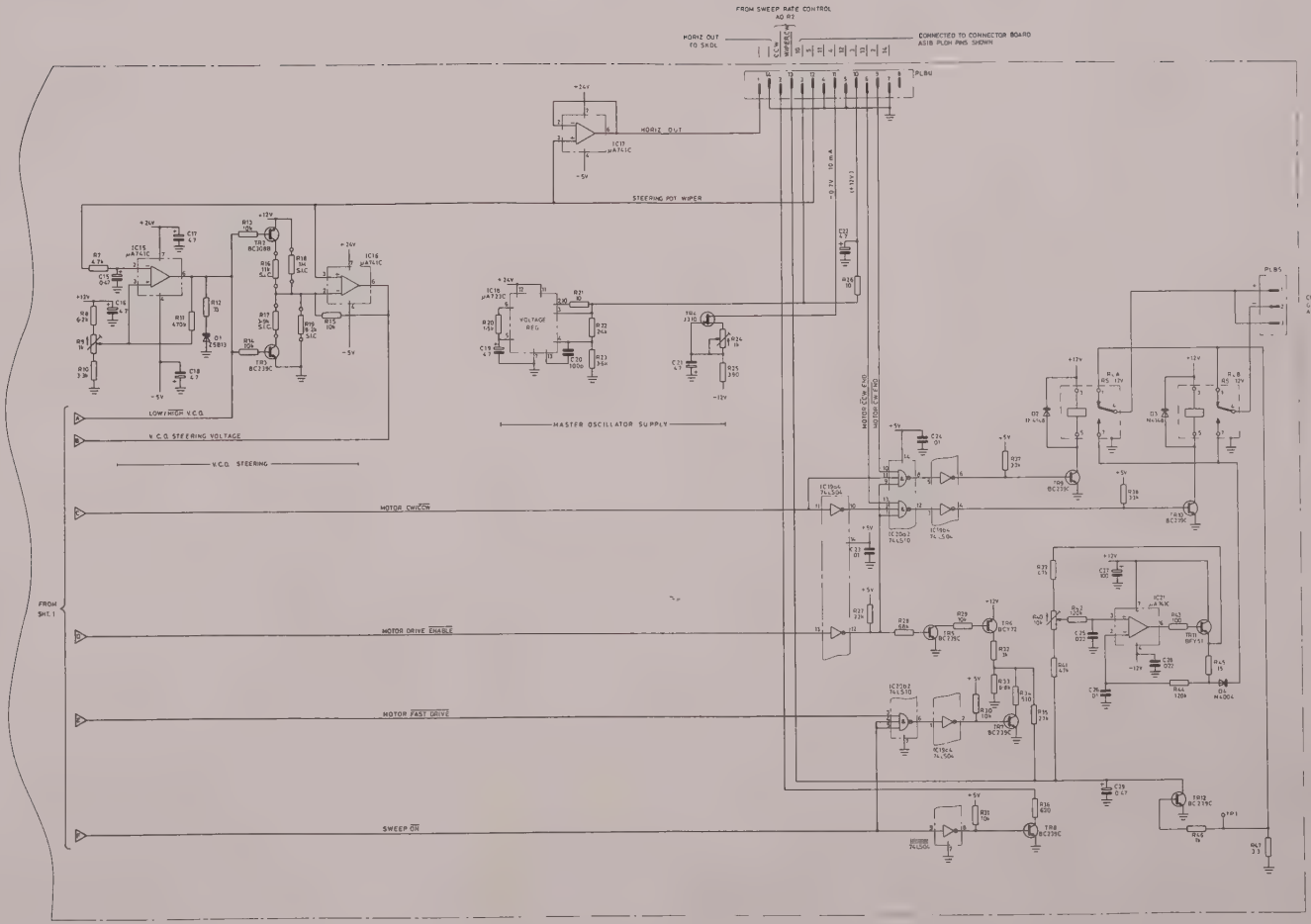

Z44828-7057 Sh.2 Iss.1

Fig. 25

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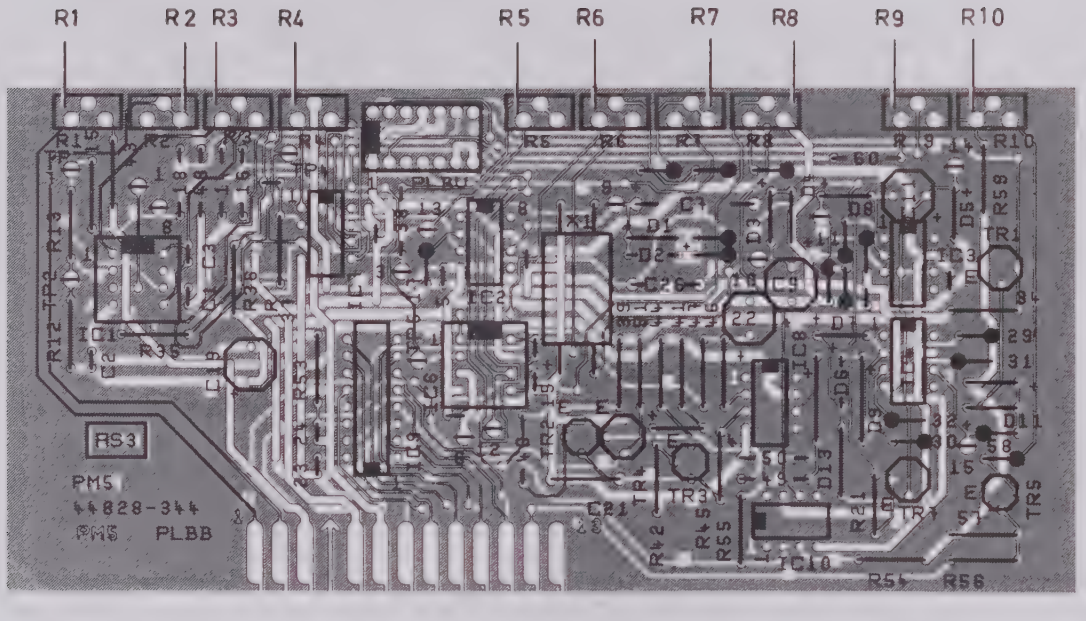
Latches, AS2, circuit diagram, sheet 2



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Component layout, AS3

Fig. 26a

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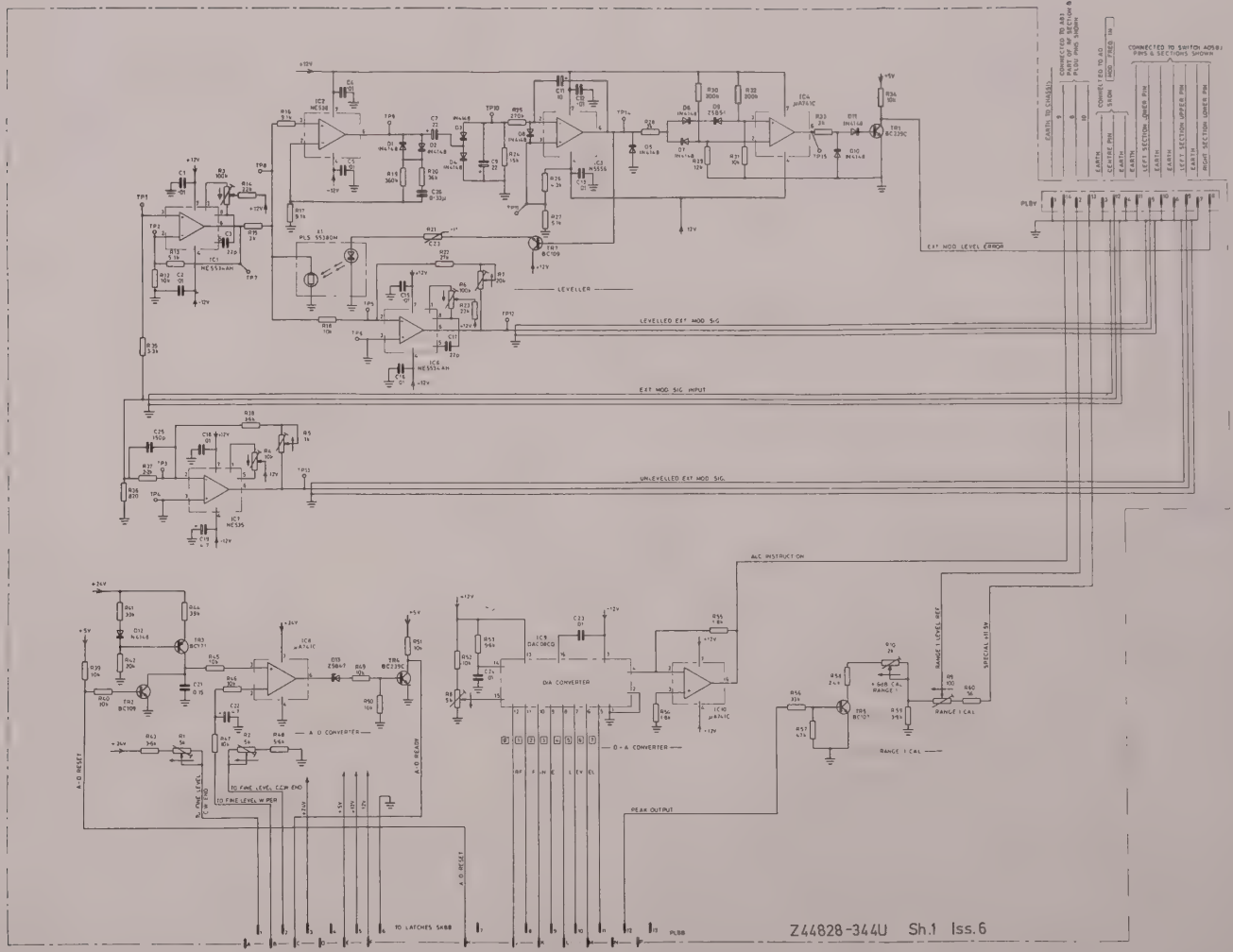
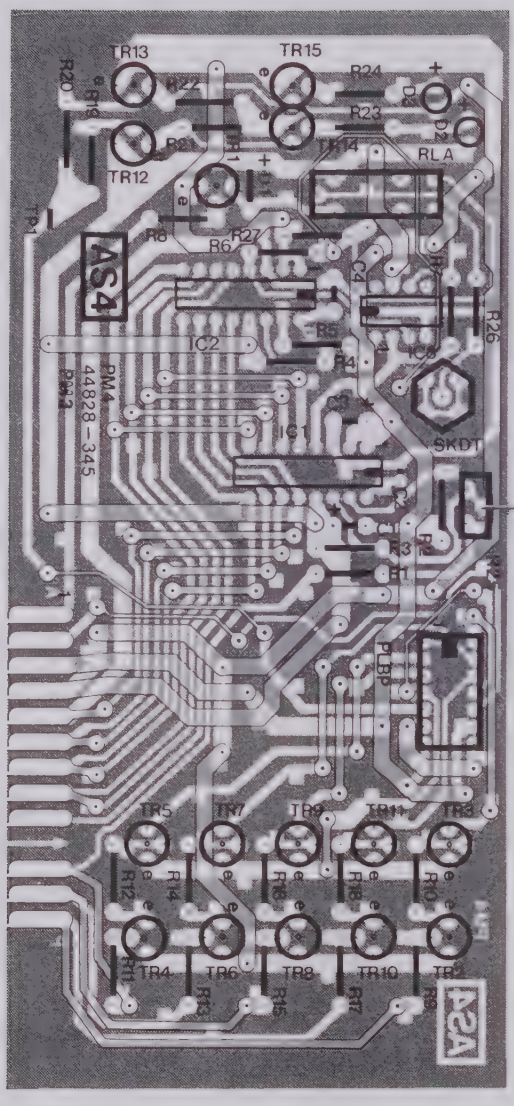


Modulation leveller, AS3, circuit diagram



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Component layout, AS4

Fig. 27a

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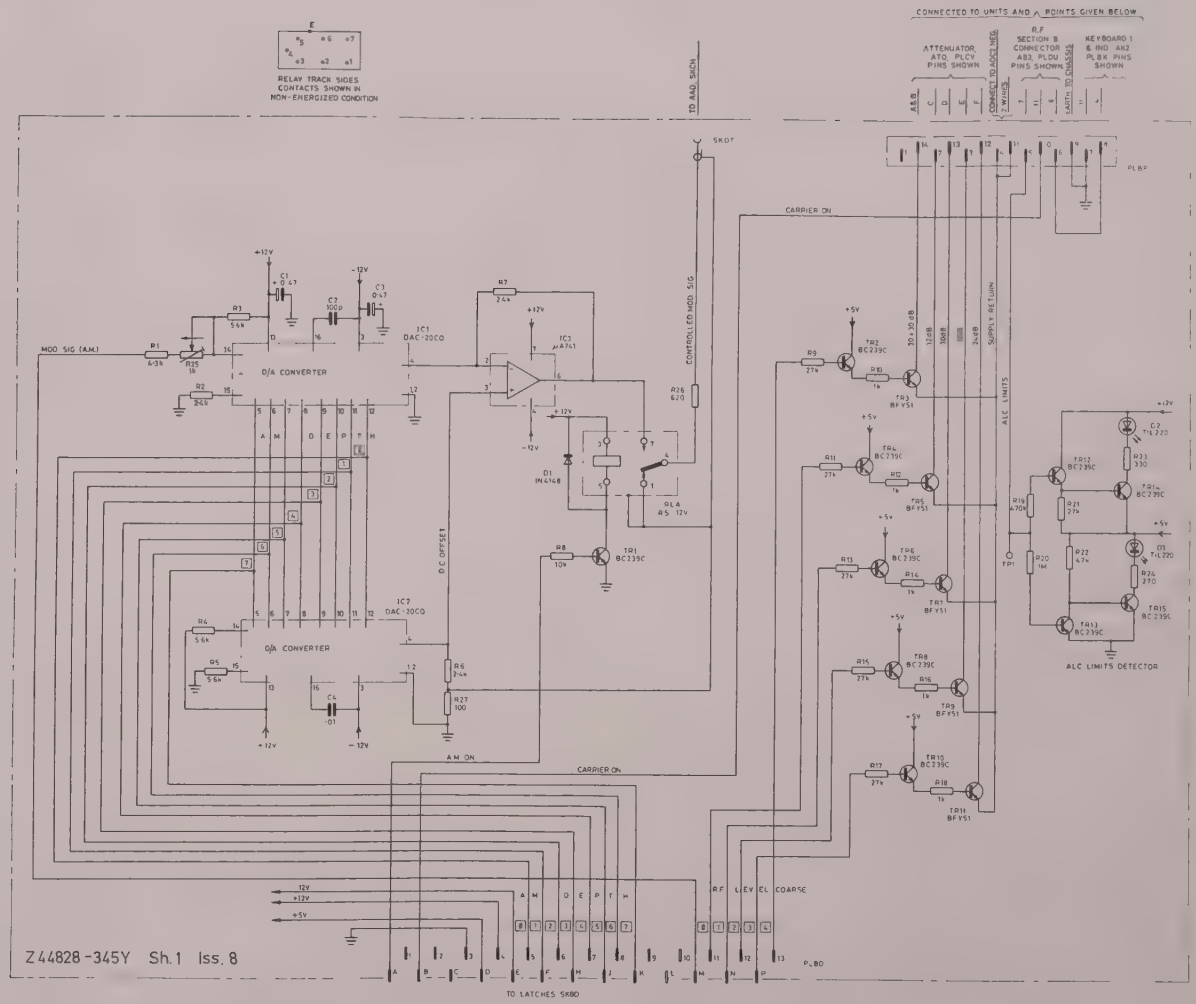

Fig. 27

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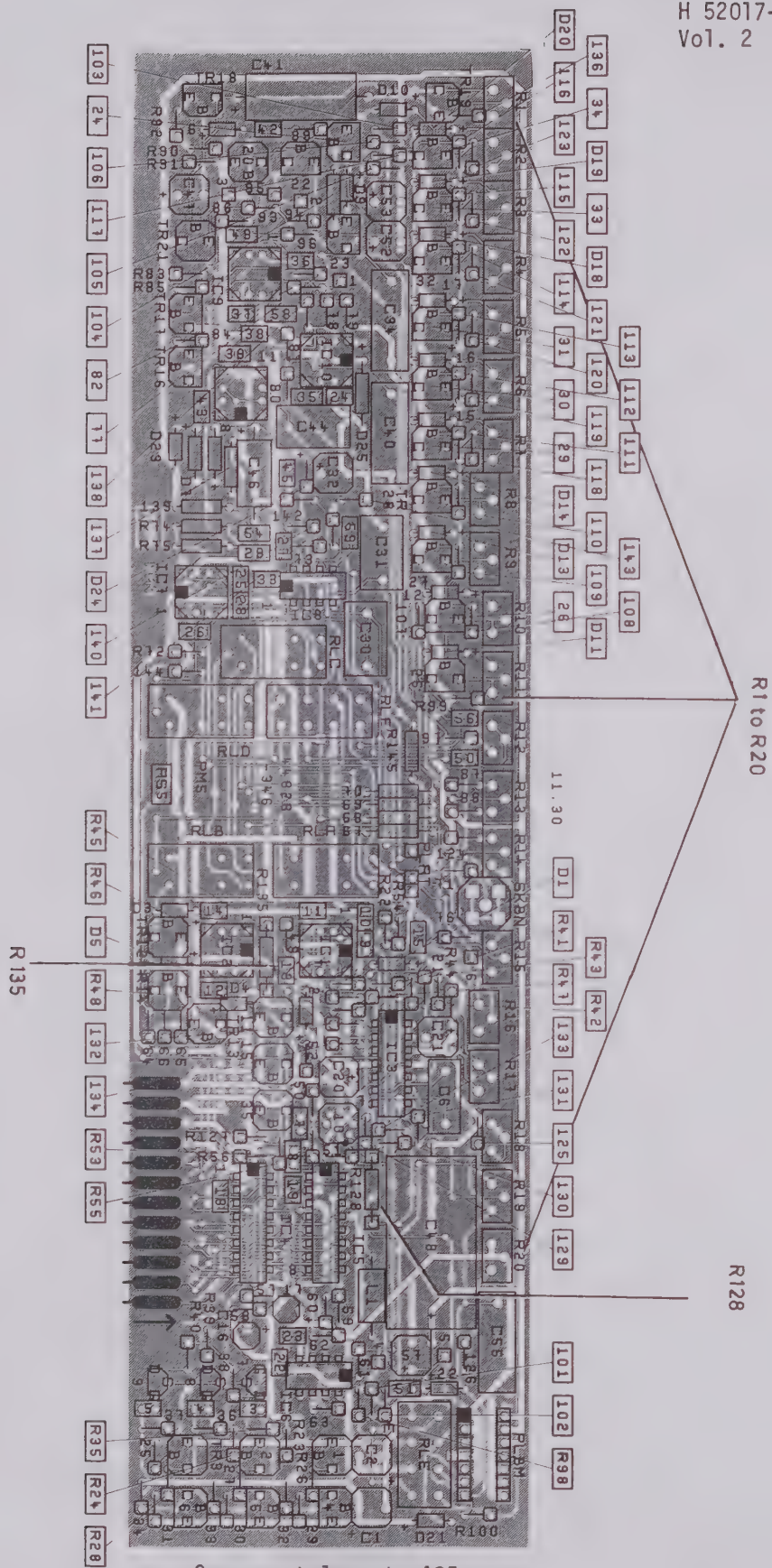
AM and attenuation control, AS4, circuit diagram



Component layout, AS5

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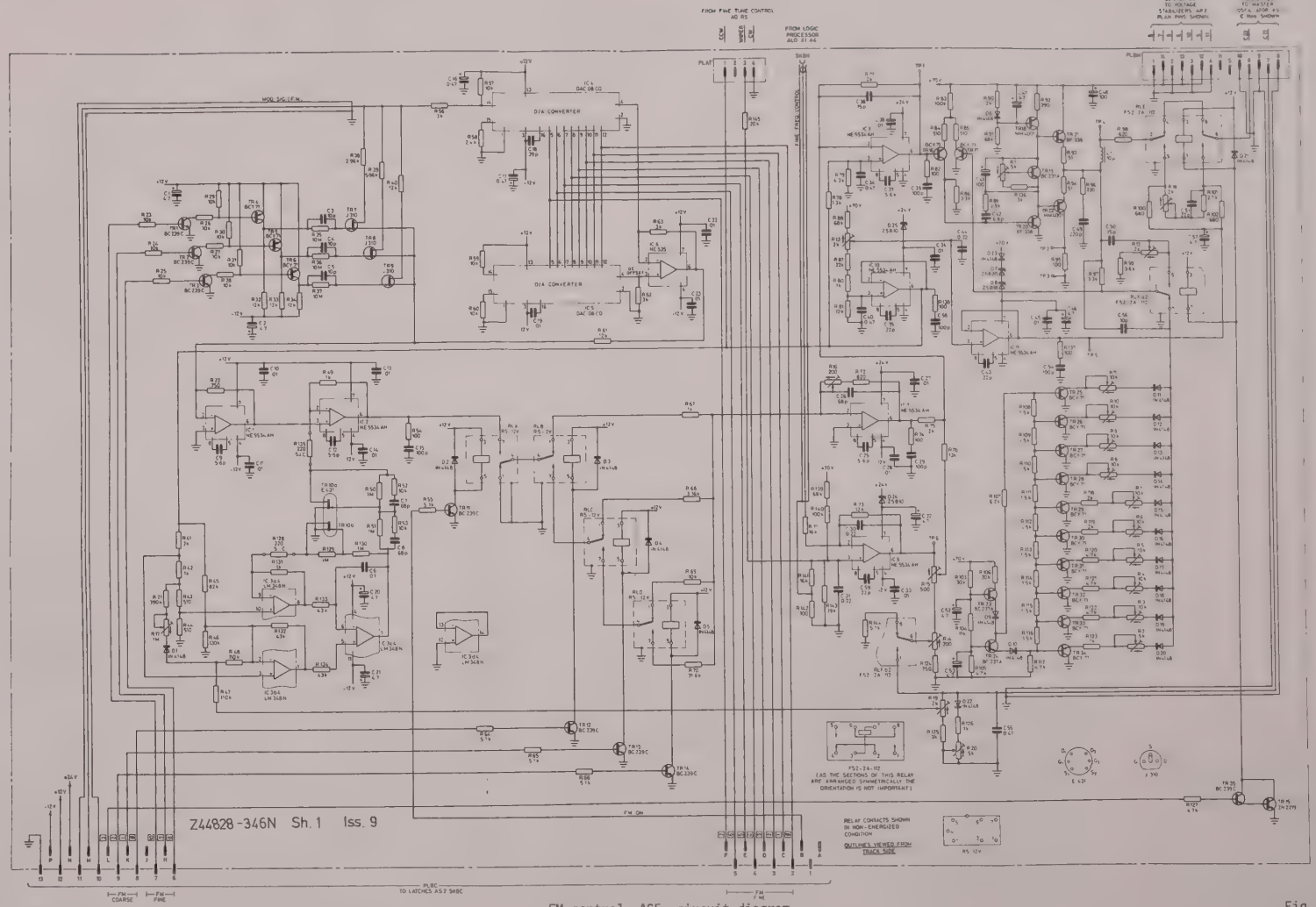

Fig. 28

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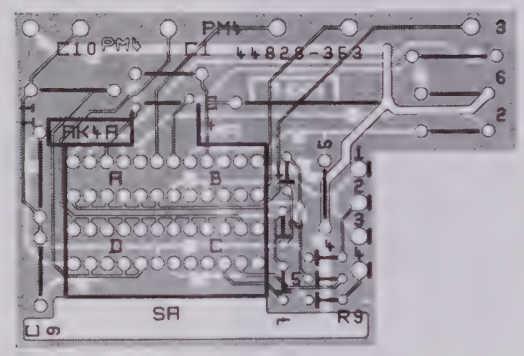

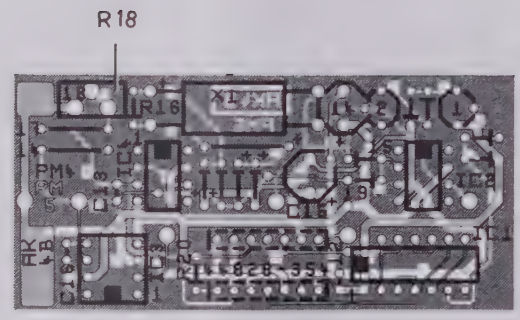

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Component layout, AK4

Fig. 29a

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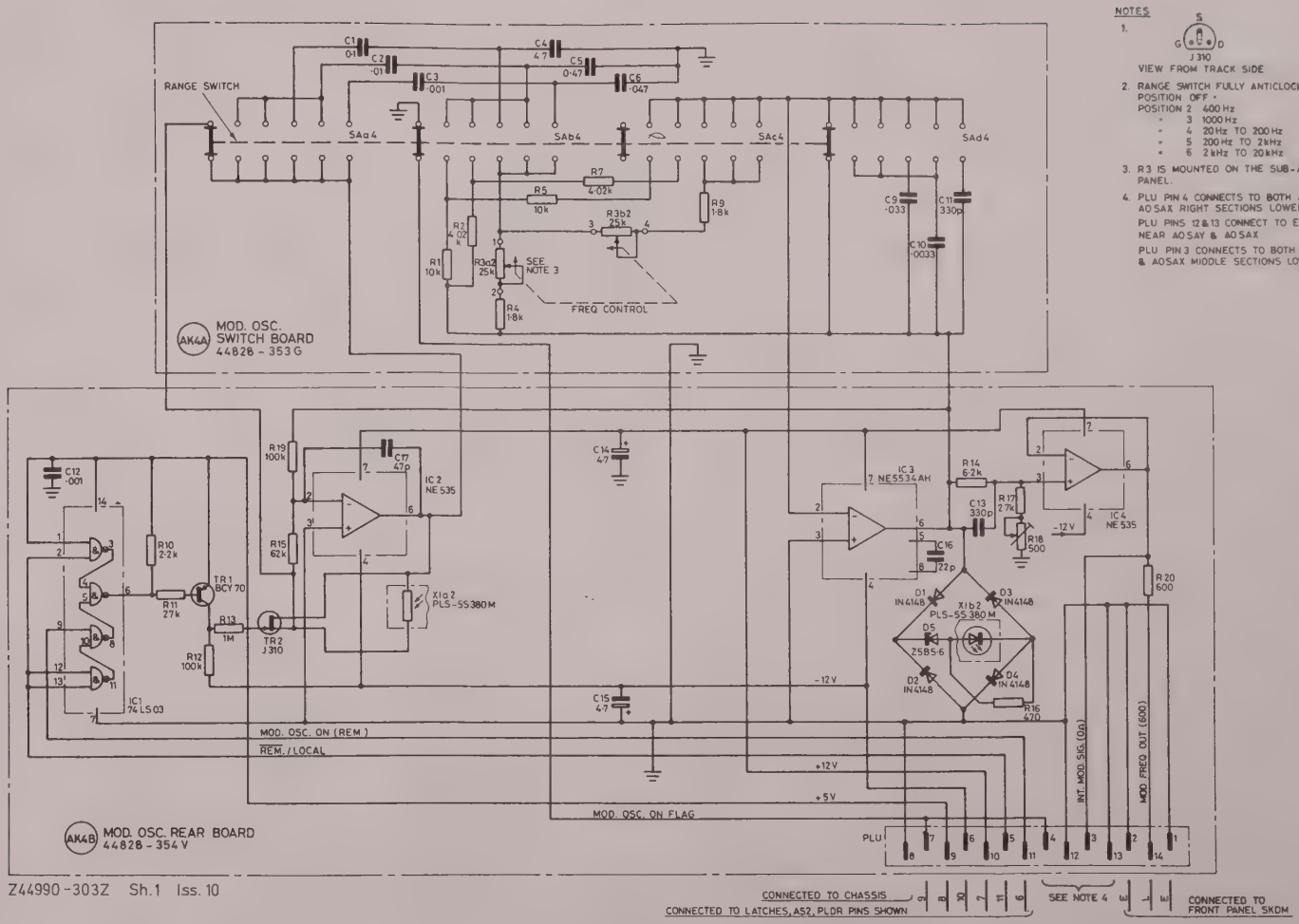

Fig. 29

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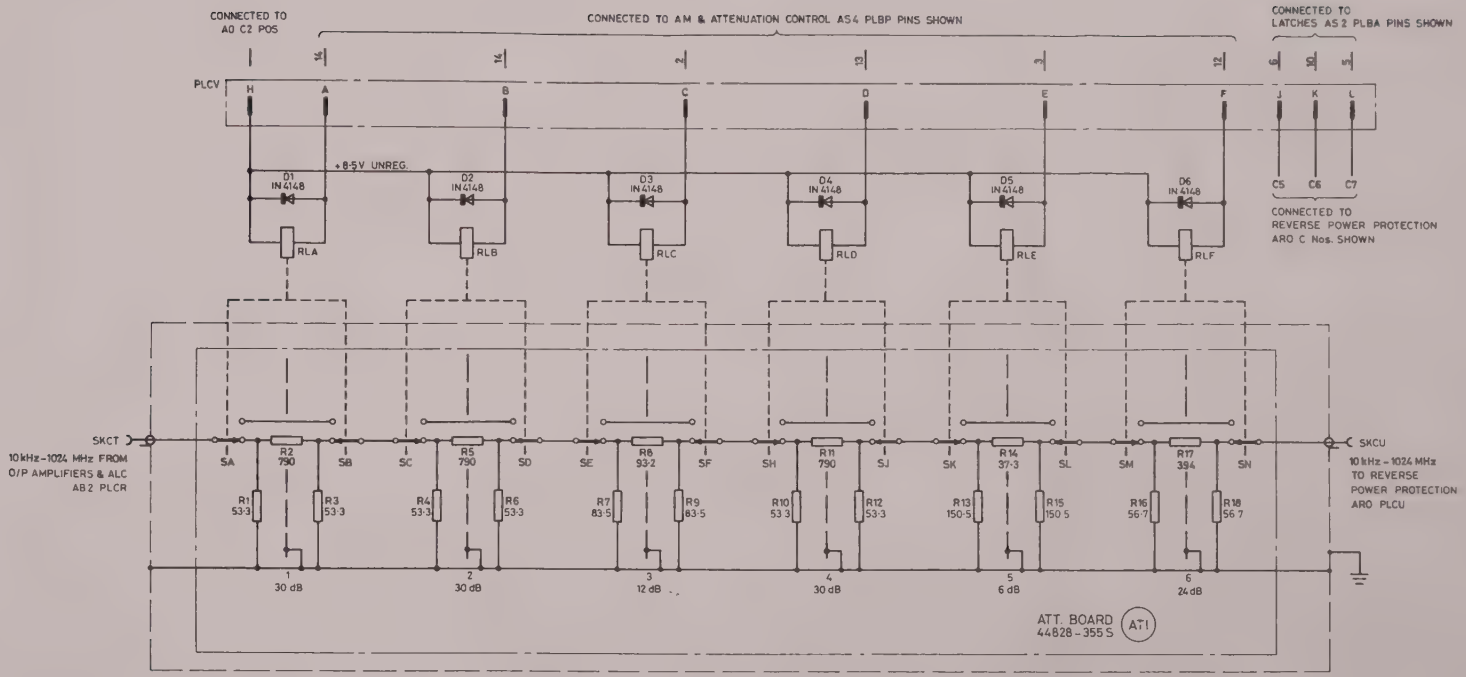
Modulation oscillator, AK4, circuit diagram comprising boards AK4A and AK4B



dB ATTENUATION			0	6	12	18	24	30	36	42	48	54	60	66	72	78	84	90	96	102	108	114	120	126	132
PADS IN CIRCUIT	1	30 dB												X	X	X	X	X	X	X	X	X	X	X	X
	2	30 dB												X	X	X	X	X	X	X	X	X	X	X	X
	3	12 dB			X	X				X	X				X	X				X	X			X	X
	4	30 dB							X		X	X	X						X		X	X	X	X	X
	5	6 dB		X		X		X	X	X	X		X	X		X		X	X	X	X		X		X
	6	24 dB					X	X		X		X	X				X	X		X		X	X	X	X

NOTE...
INSTRUMENTS WITH
Serial Nos. 118201-006 to 015
HAVE SKCU AND SKCT REVERSED

NOTE:- 1. SWITCH POSITIONS ARE SHOWN FOR RELAYS IN NON-ENERGIZED CONDITION.

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Fig. 30

Attenuator, AT0, circuit diagram

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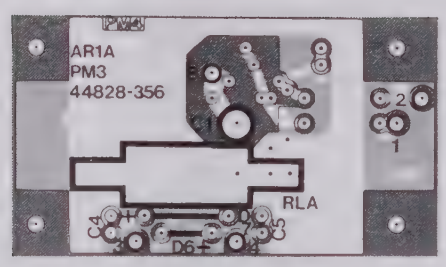

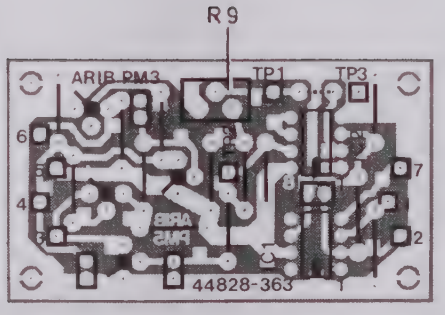

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Component layout, AR0

Fig. 31a

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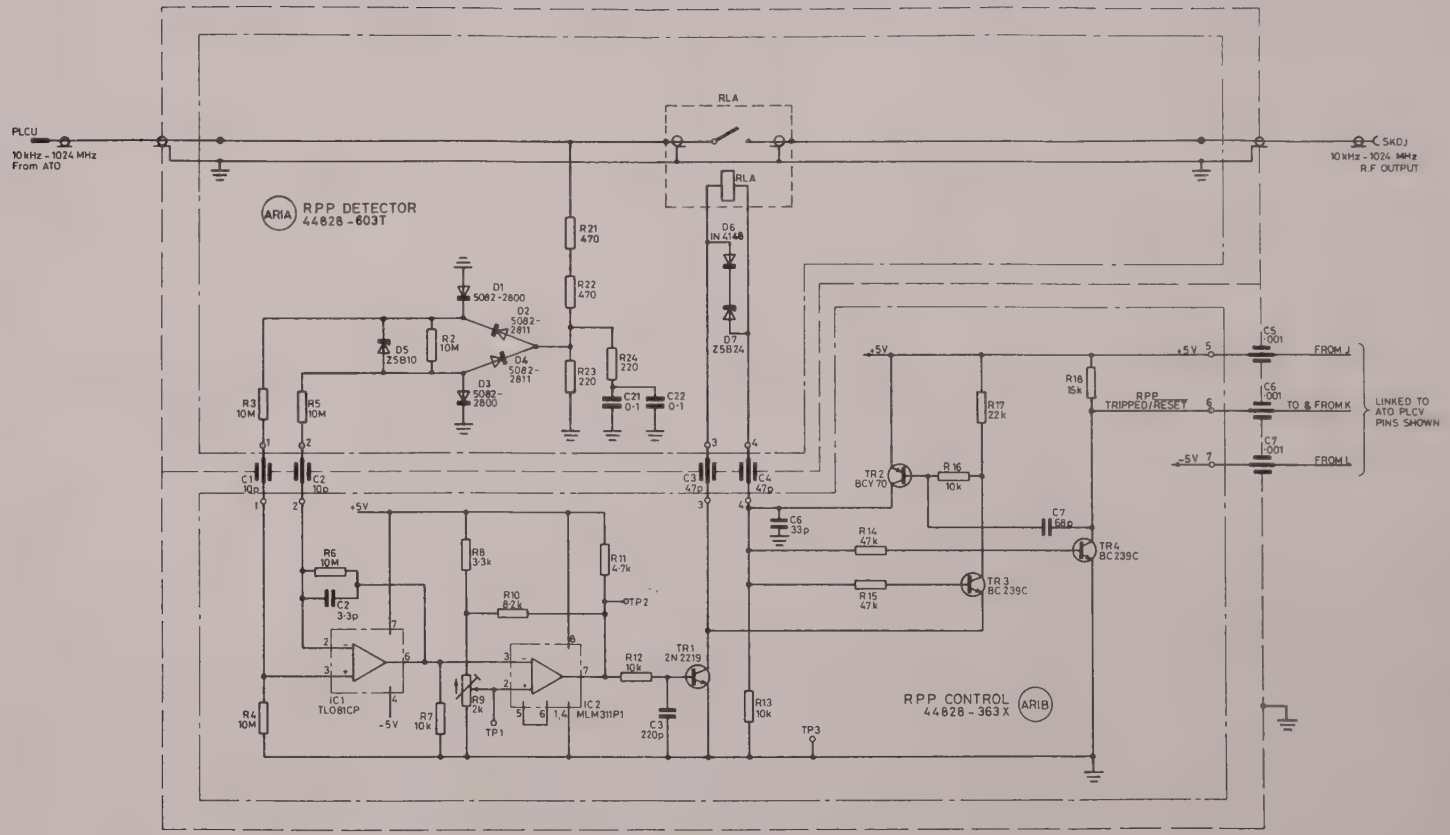

Z44990-305E Sh.1 Iss.7

NOTE:-RELAY CONTACTS SHOWN IN NON-ENERGIZED CONDITION.

Fig. 31

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Reverse power protection, ARO, circuit diagram comprising boards AR1A and AR1B

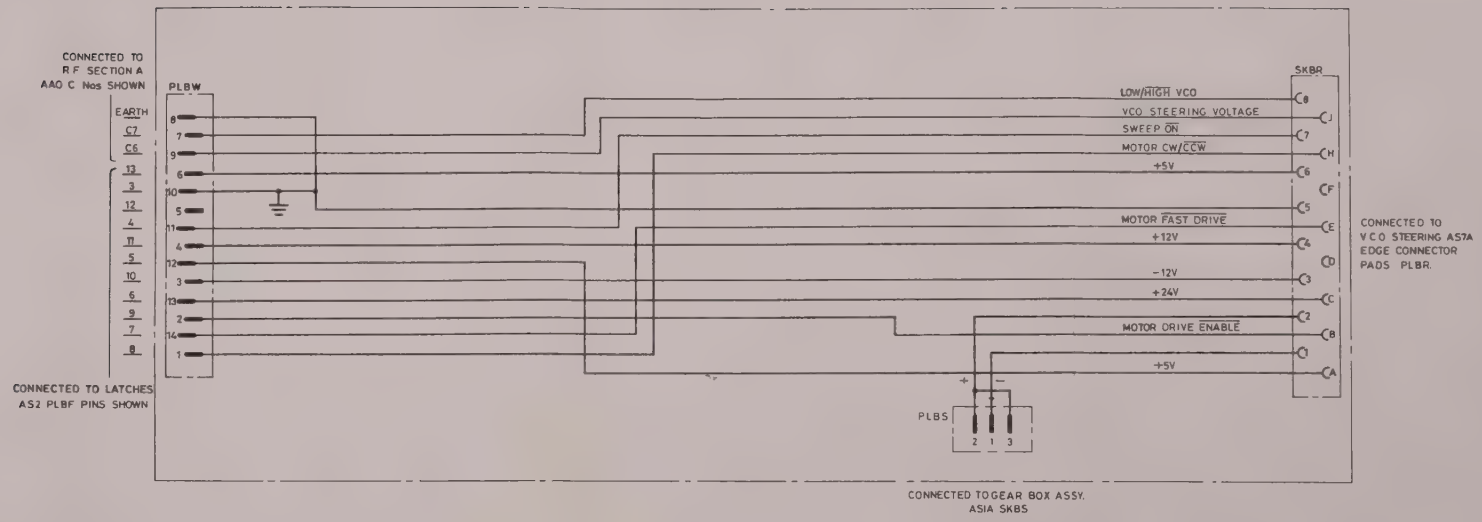

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Fig. 32

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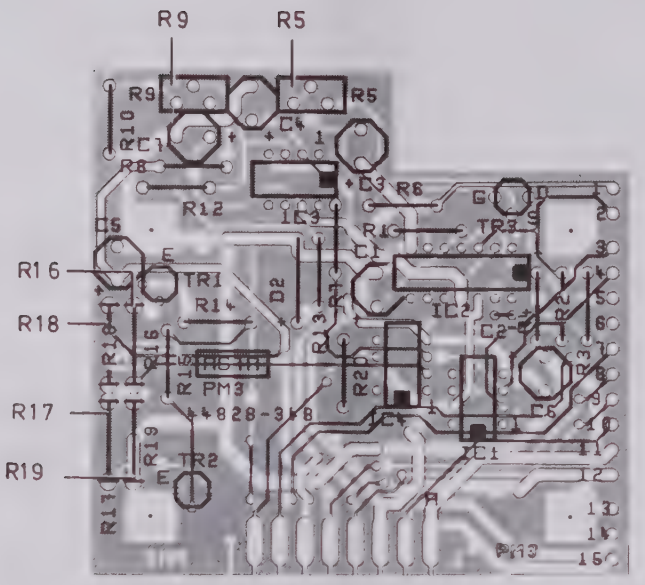
Manual/motor changeover connector board, AS6



Component layout, AS7

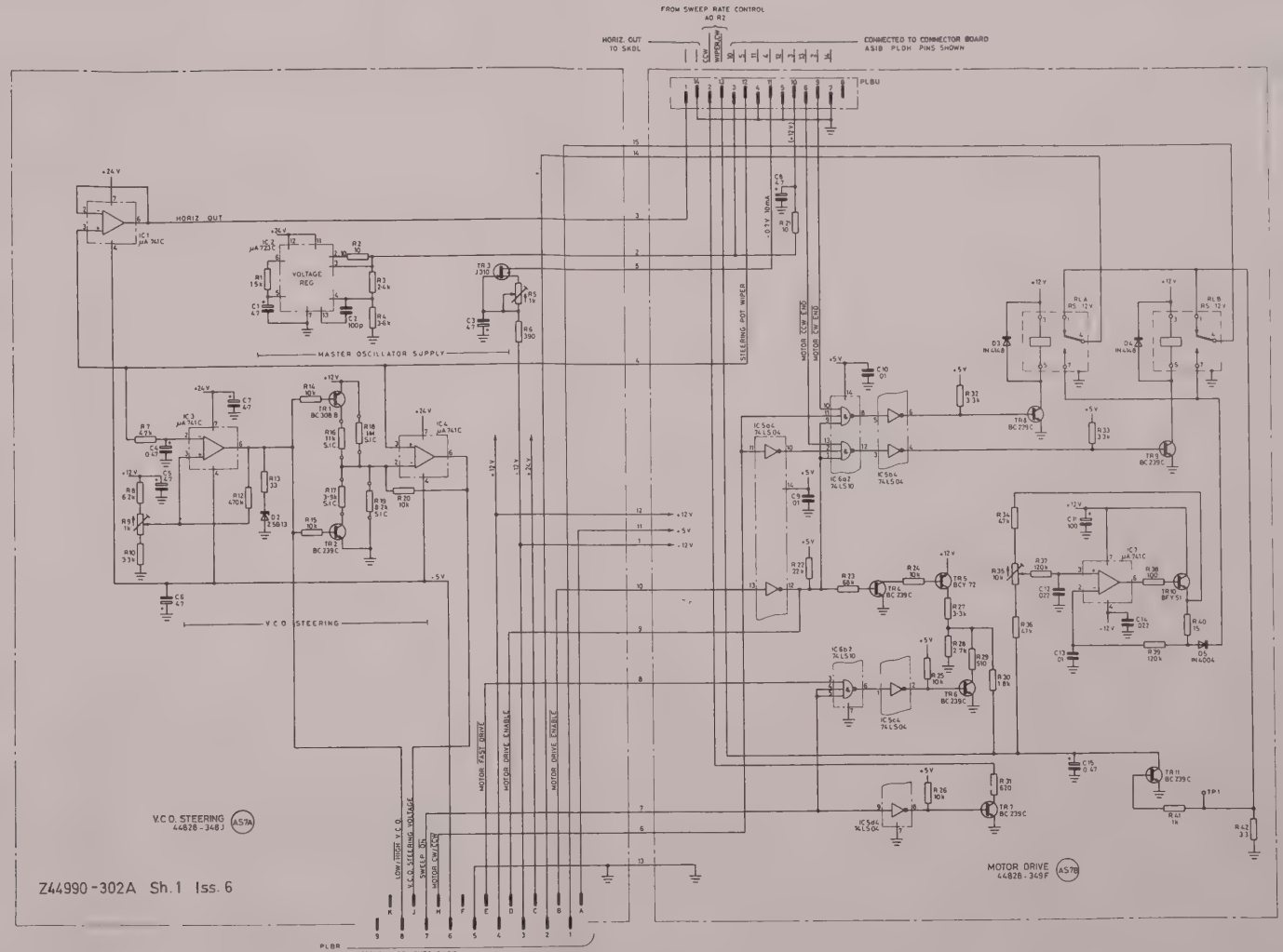


Fig. 33

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VCO steering and motor drive, AS7, circuit diagram comprising boards AS7A and AS7B

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Printed in England

EQUIPMENT 2017

TITLE ..... 10 kHz -1024 MHz
AM/FM SIGNAL GENERATOR

CODE NO. 52017-900K

SER. NOs. ..... 118201-001 to 118201-005 only

ACCOMPANYING
DOCUMENTS ..... Circuit diagram, Unit AR0

MANUAL CHANGE

Instruments with the Ser. Nos. 118201-001 to 005 have a modified Reverse power protection circuit Unit AR1A. The Service Manual should be amended as follows :-

Chap. 6 REPLACEABLE PARTS

Page 67/68 para. 45 Unit AR1A - RPP detector

Complete board should read Code 44828-356W

Delete references to C21, C22 and replace these by:

C1	Var trimmer 0.2-1.2pF	Code 26877-003B
C4	Cer 33pF 5% 63V	Code 26343-471Y
C5	Cer 33pF 5% 63V	Code 26343-471Y

Change diodes D2 and D4 to read :

Type HP 5082-2800 Code 28349-007E

Delete references to R4, R21 to R24 and amend R2 and R3 as follows :

	R2	Carb film 4.7MΩ 10% 1/8W	Code 24321-881F
	R3	Carb film 10MΩ 10% 1/8W	Code 24321-885W
Add	R5	Carb film 10MΩ 10% 1/8W	Code 24321-885W

Chap. 7 SERVICING DIAGRAMS

Page 63 Fig. 31 Reverse power protection, AR0 circuit diagram, comprising boards AR1A and AR1B (44828-603T)

Replace existing AR1A circuit by the Circuit Diagram 44828-356W included as part of AR0 44990-305E.

MARCONI INSTRUMENTS LIMITED
St. Albans, Hertfordshire, England.

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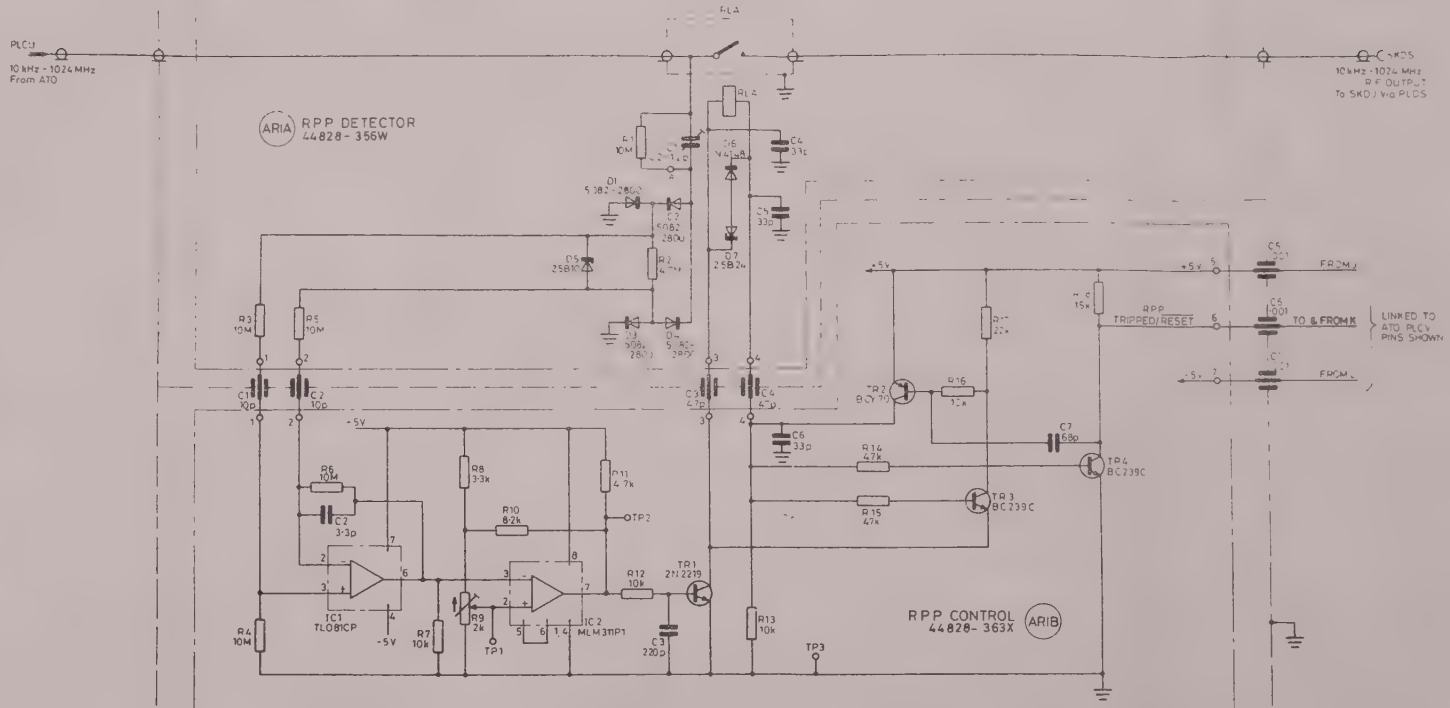
REDRAWN WITHOUT ALTERATION
L.O. 29/1/80



Applicable to Instruments Ser. No. 118201-001 to 118201-005 only

ARIA ARIB

NOTE:- RELAY CONTACTS SHOWN IN NON-ENERGIZED CONDITION.

CHECKED / /	TITLE REVERSE POWER PROTECTION (ARO)	CIRCUIT NUMBER SH 1 OF 1 SHTS Z4490-305E.	
TRACED 29/1/80 LDIX	MARCONI INSTRUMENTS LIMITED ST ALBANS ENGLAND		ISO A 4
DRAWN 11/9/78 R.P.			

EQUIPMENT 2017

TITLE ..... 10 kHz-1024 MHz
AM/FM SIGNAL GENERATOR

CODE No. 52017-900K

SER. NOs.
PREFIXED 118201

ACCOMPANYING
DOCUMENTS ..... CIRCUIT DIAGRAMS (9 off)

MANUAL CHANGE

The accompanying documents included in this Manual Change are those that differ from the published Servicing diagrams in Chapter 7 of the Service Manual Vol. 2. Only instruments with serial numbers in the series 118201 are affected. If this is applicable, replace the following figures from Chapter 7 by those included with this Manual Change.

Fig.	Unit	Title	Page
5	A0	AC pre-regulator and mains selector AP1, voltage stabilizers AP2, circuit diagram.	11
8	AL2	Display drive, circuit diagram, sheet 1	17
9	AL2	Display drive, circuit diagram, sheet 2	19
13	AG1	GPIB drive, circuit diagram	27
16	AA21	Amplitude modulator, circuit diagram	33
17	AA22	RF sub-unit 'A', circuit diagram comprising boards AA23, AA24, AA25 and AA26	35
20	AB1	10 kHz-4 MHz processing, circuit diagram	41
21	AB2	Output amplifiers and ALC, circuit diagram	43
26	AS3	Modulation leveller, circuit diagram	53

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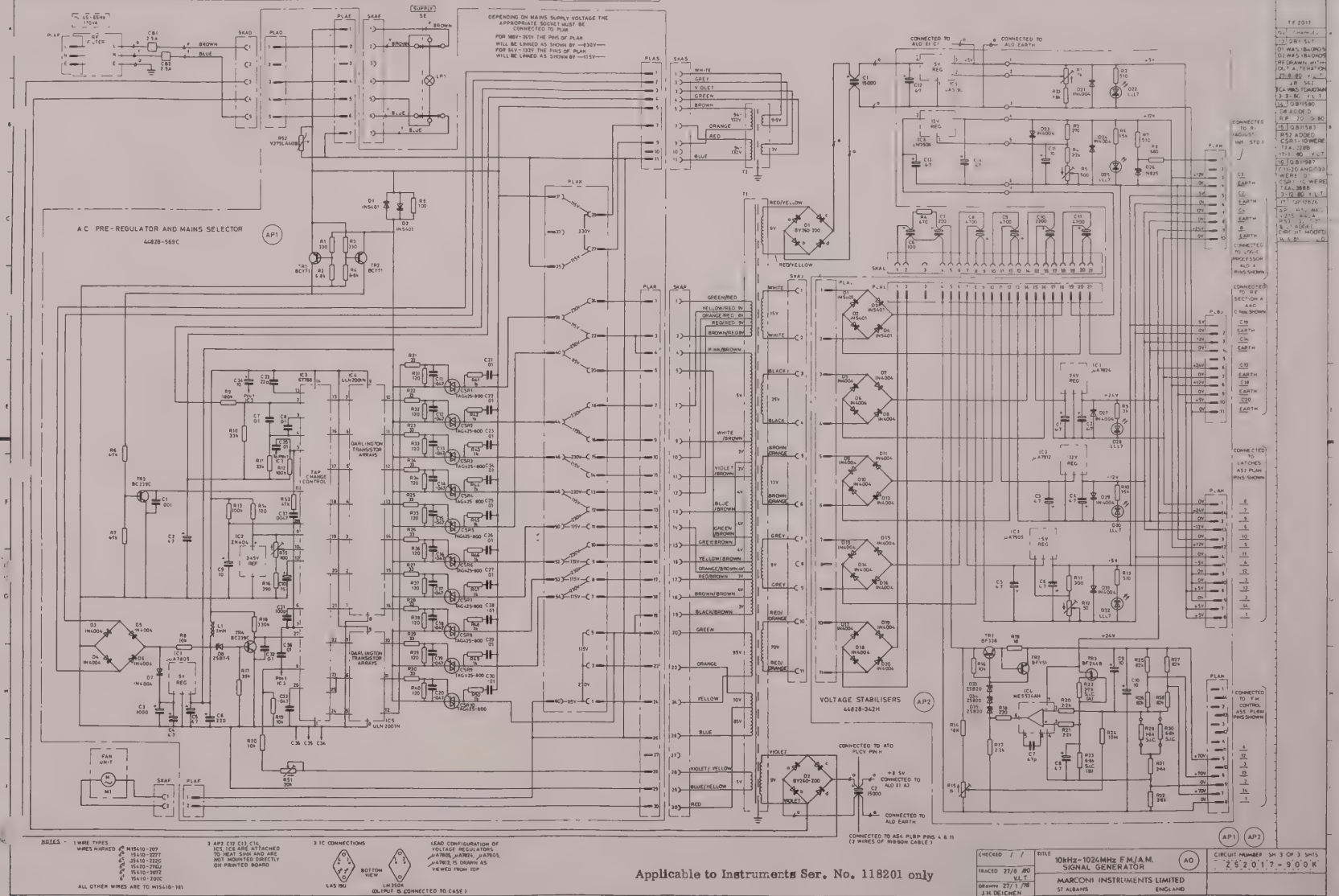
A.C. PRE-REGULATOR AND MAINS SELECTOR
44828-569C
VOLTAGE STABILISERS
44828-342H
DEPENDING ON MAINS SUPPLY VOLTAGE THE APPROPRIATE SOCKET MUST BE CONNECTED TO PLAN
FOR 185V - 265V THE PINS OF PLAN WILL BE LINKED AS SHOWN BY ——230V——
FOR 94V - 132V THE PINS OF PLAN WILL BE LINKED AS SHOWN BY ——115V——
DARLINGTON TRANSISTOR ARRAYS
TAP CHANGE CONTROL
FAN UNIT
CONNECTED TO ALO EARTH
CONNECTED TO ATO PLOY PIN H
CONNECTED TO ALO 81 A7
CONNECTED TO ALO EARTH
CONNECTED TO AS4 PLBP PINS 4 & 11 (2 WIRES OF RIBBON CABLE)
CONNECTED TO R.F. MODULATION CONTROL ASS PLAN PINS SHOWN
CONNECTED TO VISUAL PROCESSOR ALO 4 PINS SHOWN
CONNECTED TO VF SECTION A ASO C PINS SHOWN
CONNECTED TO LATCHES A57 PLAN PINS SHOWN
CONNECTED TO R. MODULATION INT STD
REDYELLOW
REDYELLOW
SUPPLY SE
BROWN
BLUE
LR1
SKAS
SKAE
SKAD
PLAS
PLAE
PLAD
SKAF
PLAF
SKAP
PLAP
SKAJ
PLAJ
SKAL
PLAL
PLAH
PLAR
WHITE
GREY
V.OLET
GREEN
BROWN
ORANGE
RED
BLUE
YELLOW
VIOLET
GREEN/RED
YELLOW/RED IN
ORANGE/RED IN
RED/RED IN
BROWN/RED IN
P.INK/BROWN
BLACK
WHITE/BROWN
VIOLET/BROWN
BLUE/BROWN
GREEN/BROWN
GREY/BROWN
YELLOW/BROWN
ORANGE/BROWN
RED/BROWN
BROWN/BROWN
BLACK/BROWN
GREEN
ORANGE
YELLOW
BLUE
VIOLET/YELLOW
BLUE/YELLOW
RED
VIOLET
REDU ORANGE
GREY
BROWN ORANGE
BLACK
WHITE
+5V
+12V
+24V
-5V
-12V
+70V
0V
+8.5V
CB1 2.5A
CB2 1.5A
RF FILTER
TR1 BC171
TR2 BC171
TR3 BC239C
TR4 BC239C
TR5 BC239C
TR6 BC239C
TR7 BF338
TR8 BF451
TR9 BF348
TR10 BF348
IC1 LM350K
IC2 ZN404
IC3 67766
IC4 ULN2004
IC5 ULN2001N
IC6 MES5164
IC1 μA7824
IC2 μA7912
IC3 μA7905
IC4 LM723CH
IC5 LM723CH
IC6 LM723CH
IC7 LM723CH
IC8 LM723CH
IC9 LM723CH
IC10 LM723CH
IC11 LM723CH
IC12 LM723CH
IC13 LM723CH
IC14 LM723CH
IC15 LM723CH
IC16 LM723CH
IC17 LM723CH
IC18 LM723CH
IC19 LM723CH
IC20 LM723CH
IC21 LM723CH
IC22 LM723CH
IC23 LM723CH

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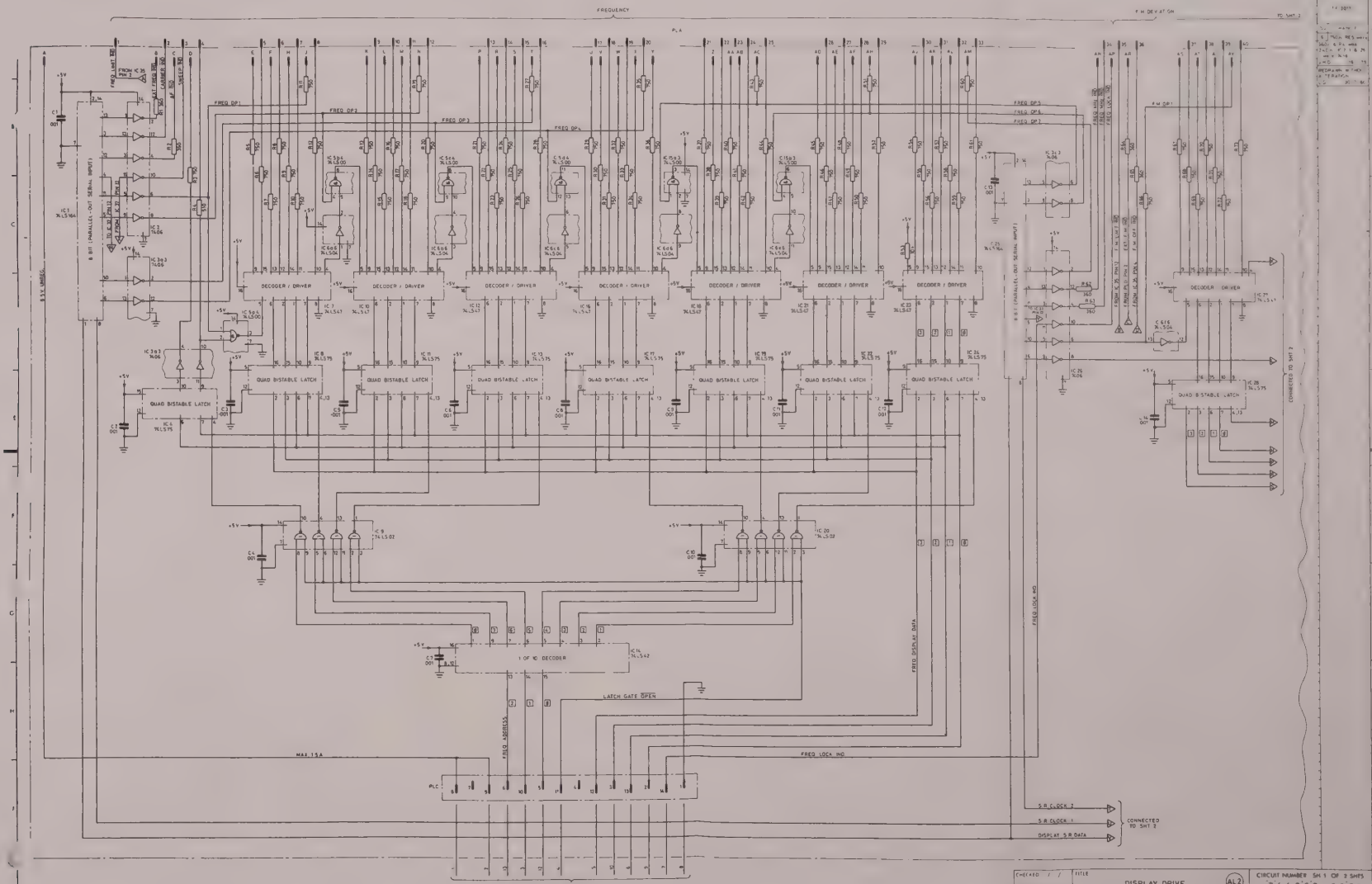

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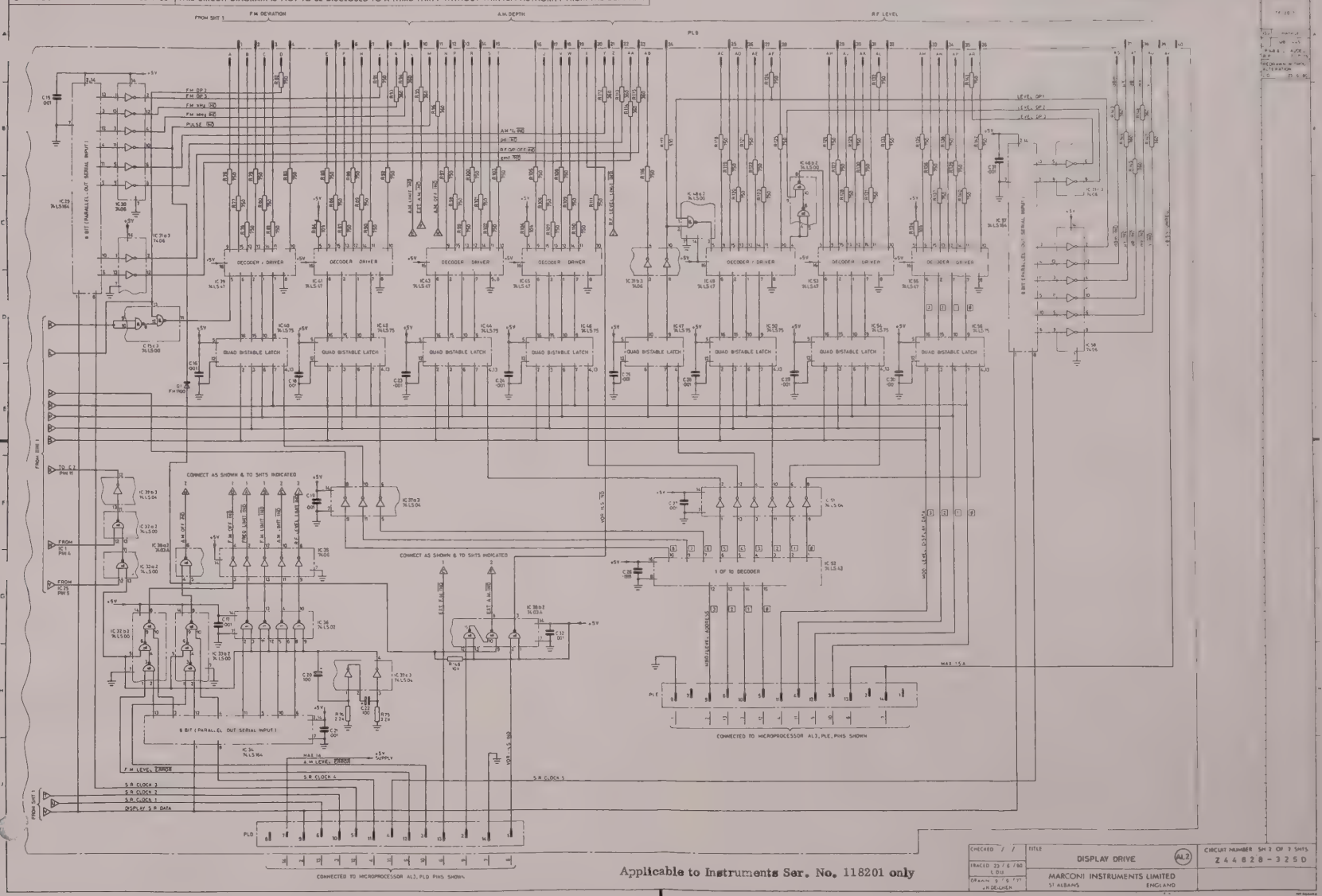

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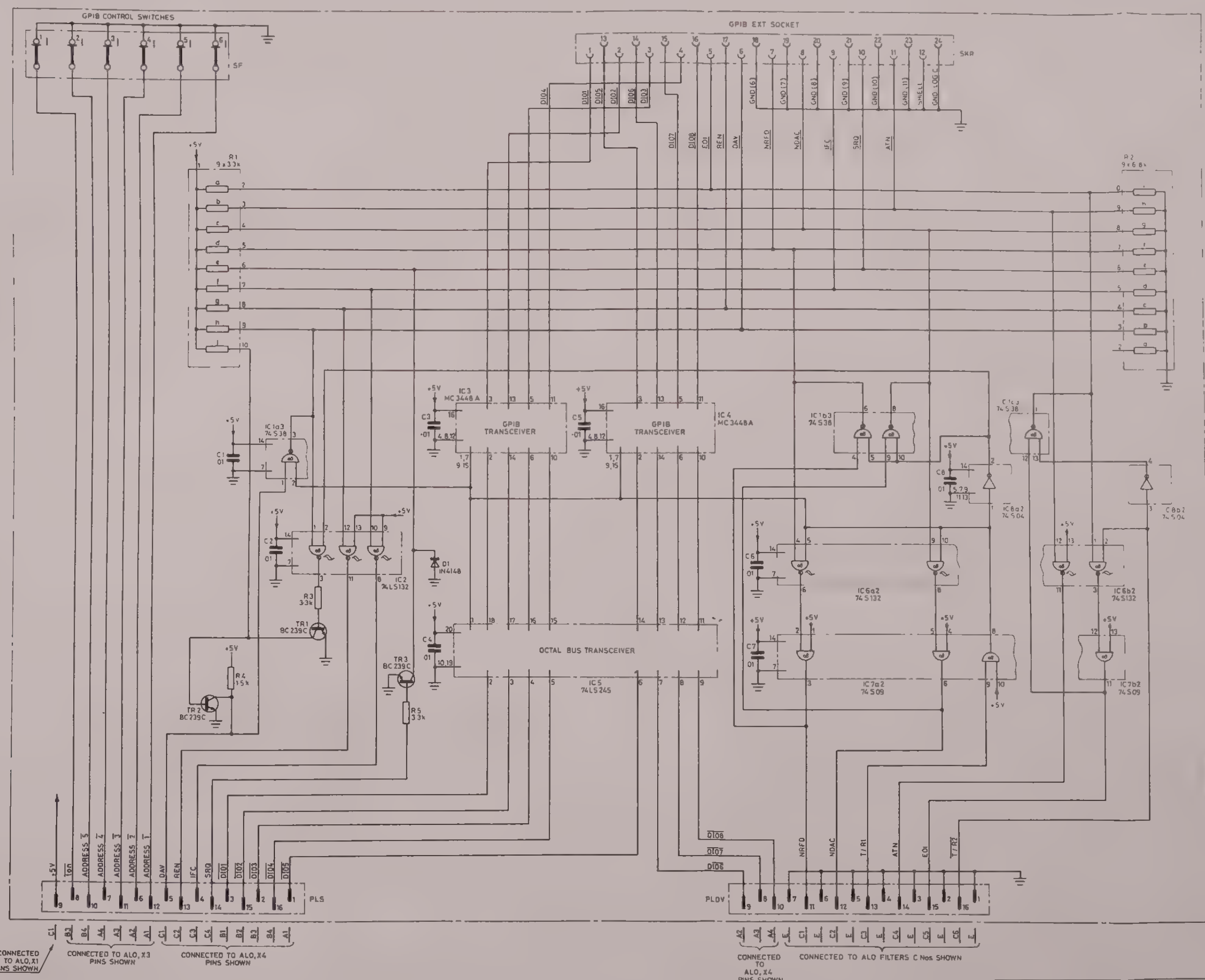

NOTES

UNDERLINED LABELS REFER TO GPIB TERMS WHICH ARE NEGATIVE TRUE
ALL OTHER LABELS ARE POSITIVE TRUE

GPIB ABBREVIATIONS

ATN ATTENTION
SRQ SERVICE REQUEST
IFC INTERFACE CLEAR
DAC DATA ACCEPTED
NDAC NOT DATA ACCEPTED
RFD READY FOR DATA
NRFD NOT READY FOR DATA
DAV DATA VALID
EOI END OR IDENTIFY
DIO DATA INPUT/OUTPUT
REN REMOTE ENABLE
ton TALK ONLY

TF 2017

ISS	CHANGE
3	OB 11467 R1&TR2 CHANGED RP 10.1.80
	REDRAWN WITH ALTERATION

Applicable to Instruments Ser. No. 118201 only

CHECKED / /	TITLE GPIB DRIVE (AG1)	CIRCUIT NUMBER SH 1 OF 1 SHTS Z44828-387S
TRACED 17/3/80 L DIX	MARCONI INSTRUMENTS LIMITED ST ALBANS ENGLAND	
DRAWN 14/5/79 J.H.DEICHEN		

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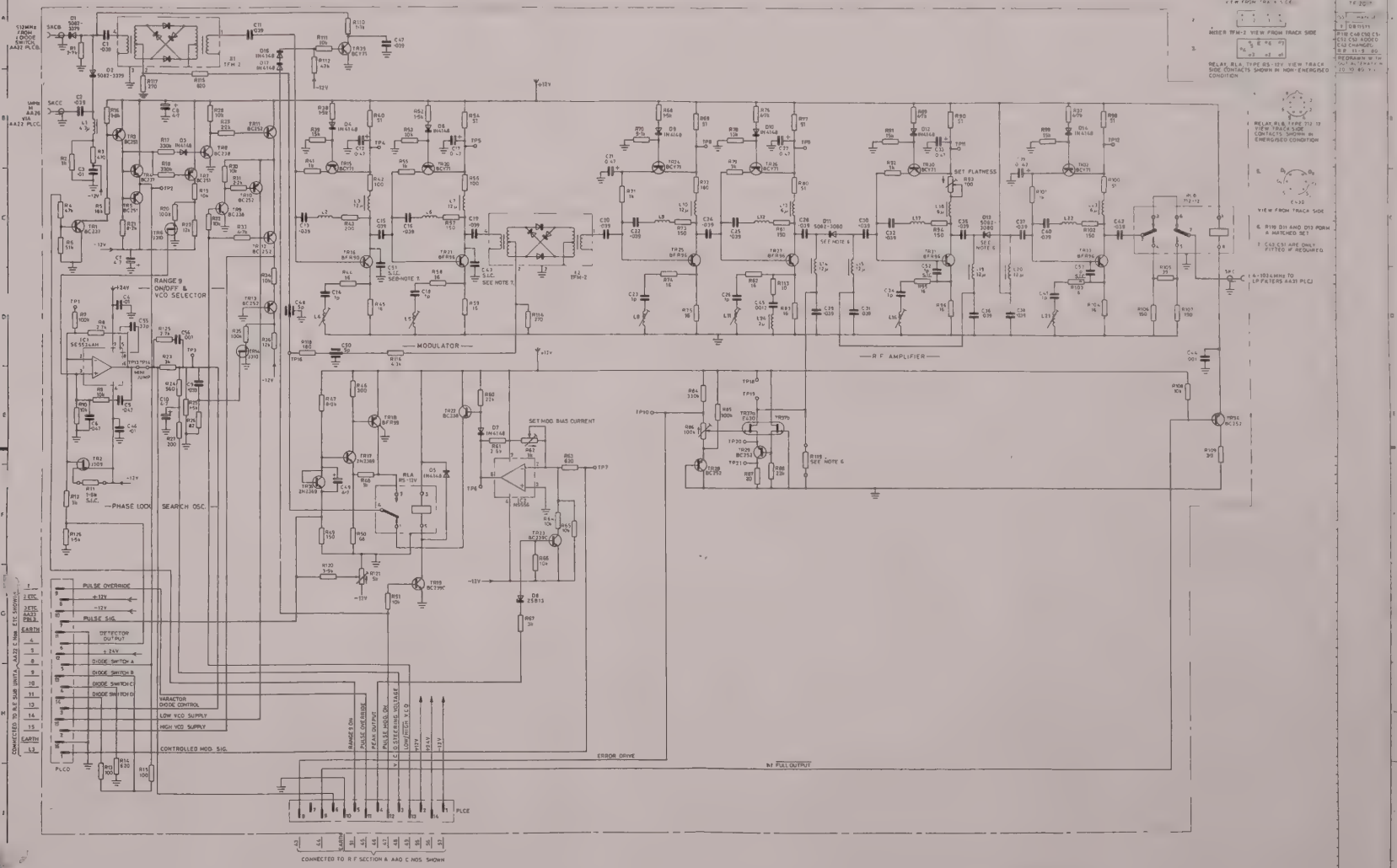

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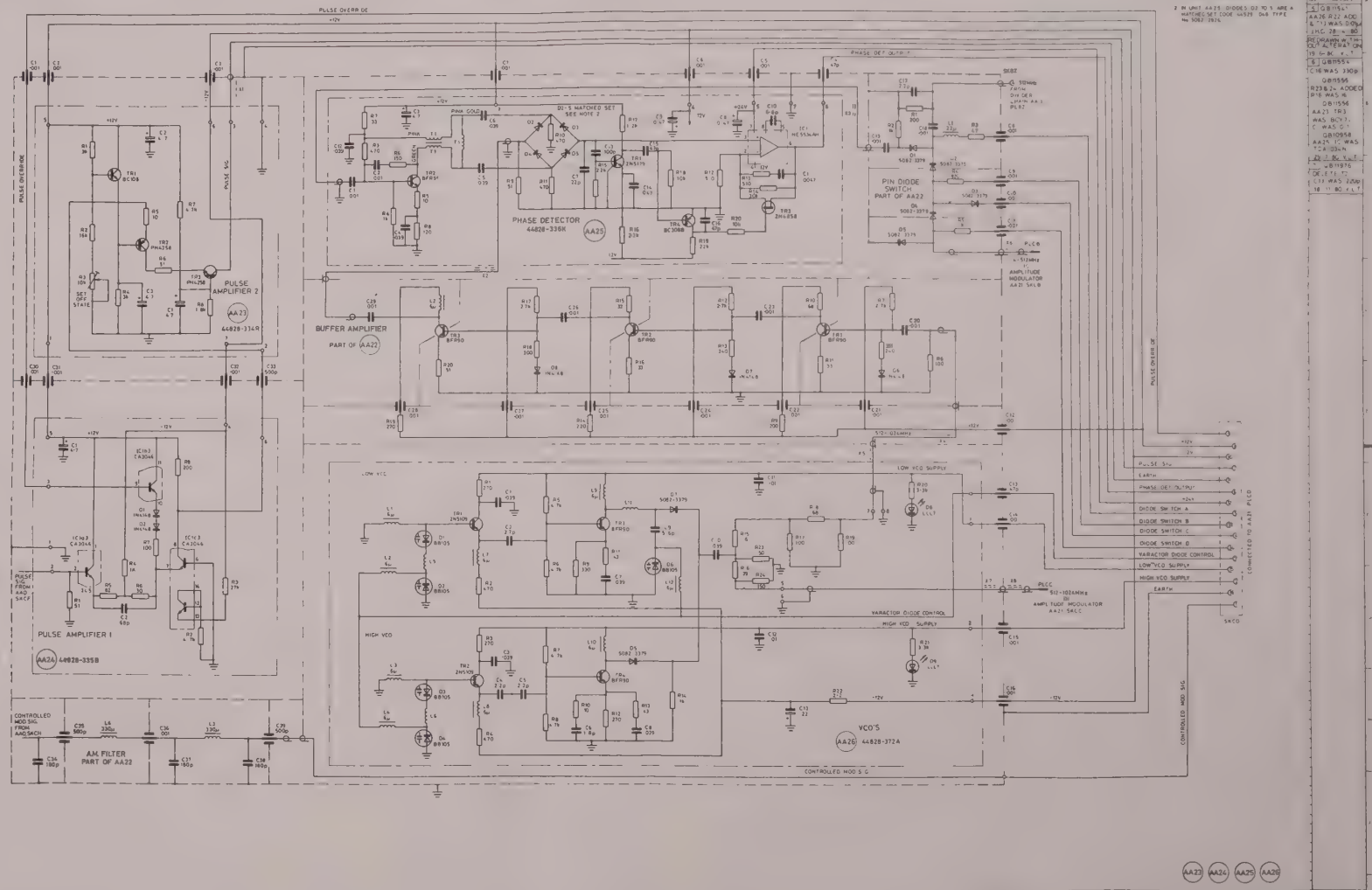

Applicable to Instruments Ser. No. 118201 only

CHECKED / /	TITLE R.F. SUB-UNIT A (AA22)	CIRCUIT NUMBER SH 1 OF 1 SHTS	
TRACED 19/6/80 VLT	MARCONI INSTRUMENTS LIMITED ST ALBANS ENGLAND	Z 4 4 9 9 0 - 2 9 8 H	
DRAWN 7/2/79 J.H. DEICHEN			

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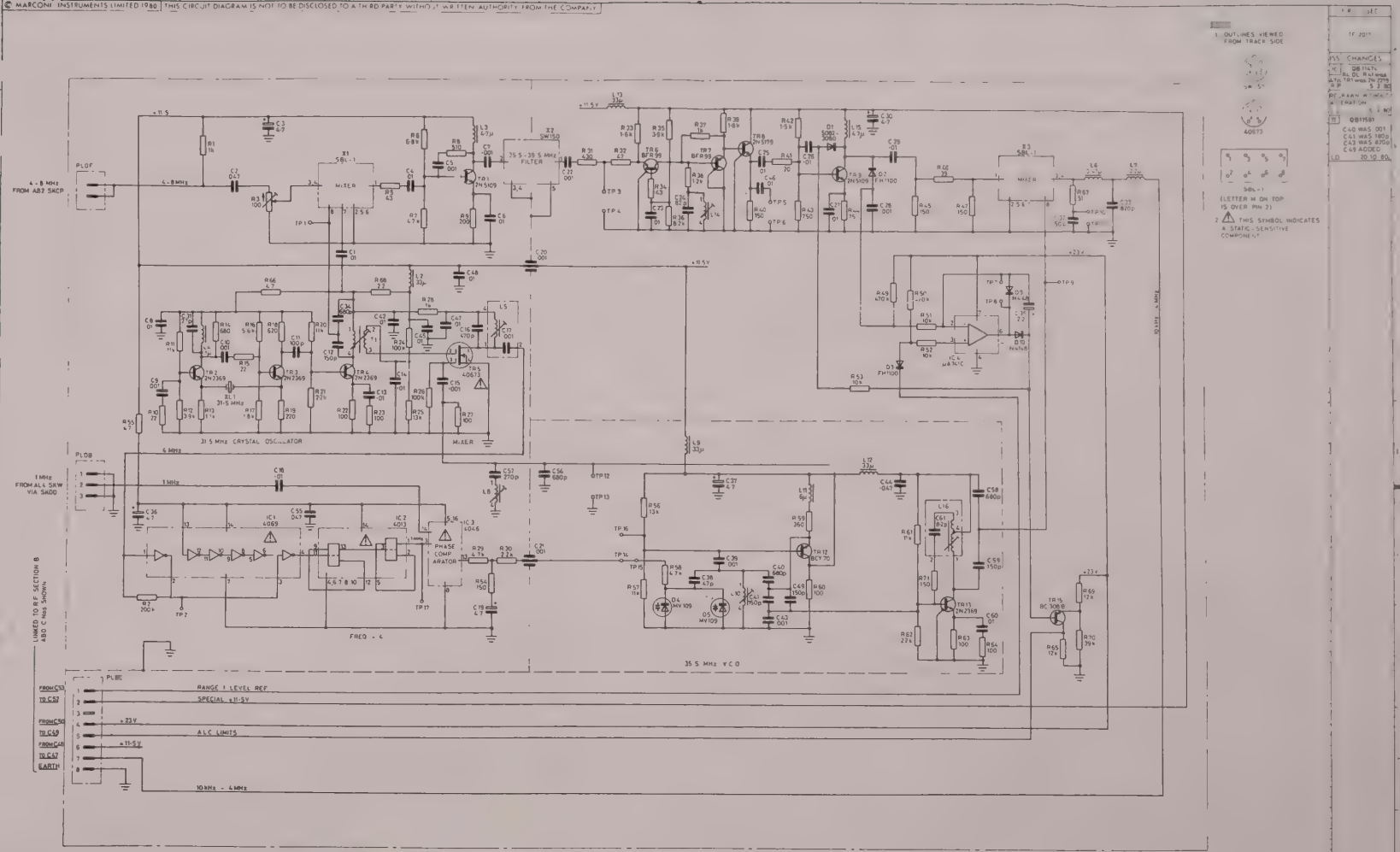

Applicable to Instruments Ser. No. 118201 only

CHECKED / /	TITLE	(AB1)	CIRCUIT NUMBER SH 1 OF 1 SHTS
TRACED 6/3/80 L DIX	10 kHz-4 MHz PROCESSING		Z448 28-33 8Z
DRAWN 24/8/79 R P	MARCONI INSTRUMENTS LIMITED ST ALBANS ENGLAND		SO A

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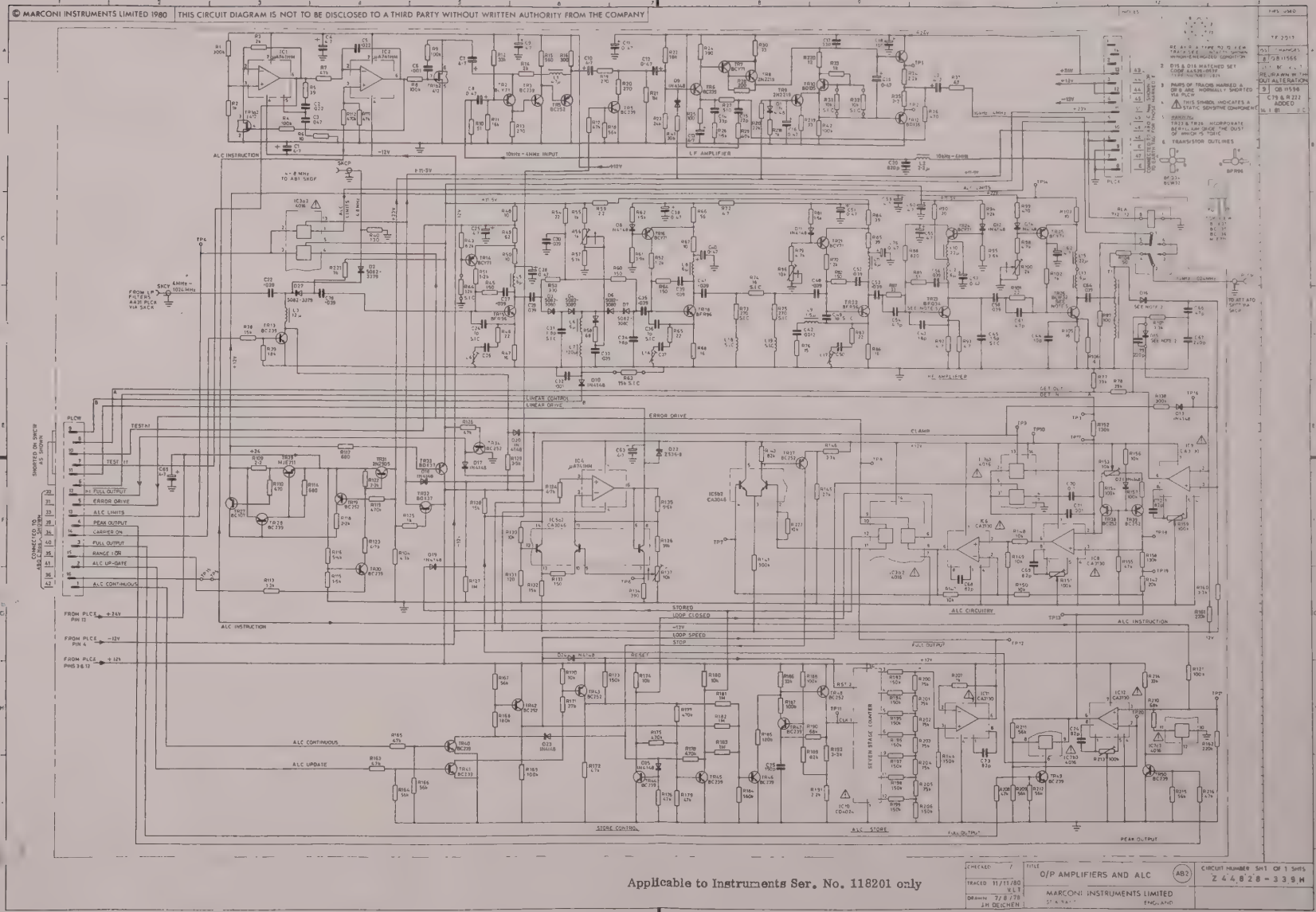

Applicable to Instruments Ser. No. 118201 only

CHECKED		TITLE	O/P AMPLIFIERS AND ALC
TRACED	11/11/80 VLT		MARCONI INSTRUMENTS LIMITED
DRAWN	7/8/78 JH DEECHEN		ENGLAND

AB2

CIRCUIT NUMBER Sht 1 OF 1 Shts
Z44828-339H

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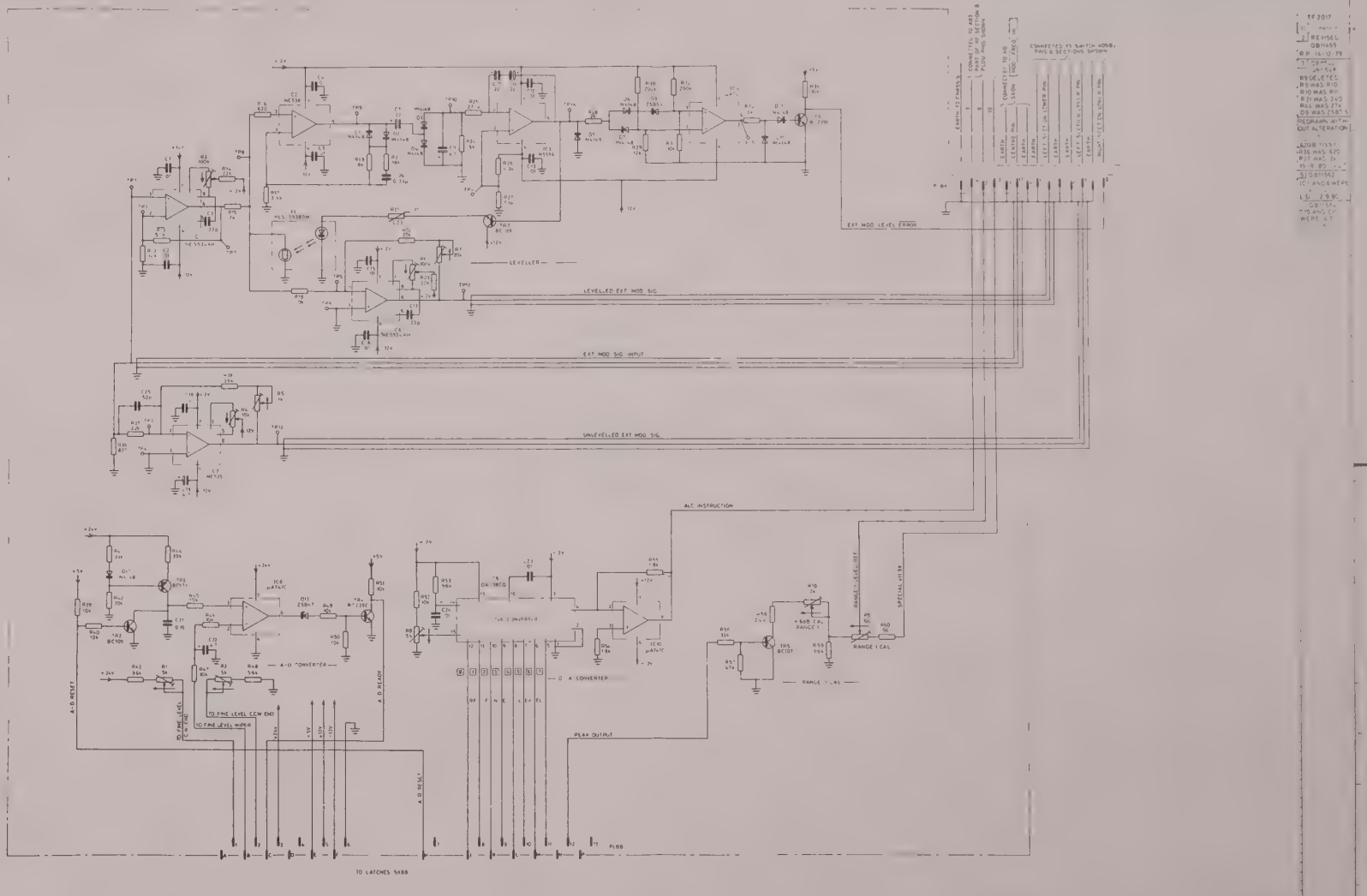

Applicable to Instruments Ser. No. 118201 only

CHECKED / /	TITLE	MODULATION LEVELLER (AS3)	CIRCUIT NUMBER SH 1 OF 1 SHTS
TRACED 31/7/80 V.L.I.		MARCONI INSTRUMENTS LIMITED ST ALBANS ENGLAND	Z 44828-344U
DRAWN 29/5/78 J.M. DEICHEN			

EQUIPMENT ... 2017

TITLE ..... 10 kHz - 1024 MHz
AM/FM SIGNAL GENERATOR

CODE No..... 52017-900K

SER. Nos..... 118201 & 118202

ACCOMPANYING
DOCUMENTS ... Circuit diagram, Unit AS2

MANUAL CHANGE

Modifications have been carried out to reduce floor noise on Amplitude Modulator board AA21, these and other minor changes are included below. Amend the Service manual as follows:-

Chap. 6 REPLACEABLE PARTS

Page 4, para. 7 Unit A0 - Chassis

Change C14 to read Elec 4.7µF -20+100% 63V	Code no. 26415-801M

Page 23, para. 21 Unit AA11 - Divider chain

Add C59 Elec 220µF -20+100% 10V	Code no. 26415-817J

Page 26, para. 22 Unit AA21 - Amplitude modulator

Change C8 to read Tant 22µF 20% 15V	Code no. 26486-230B
C21 " " Tant 4.7µF 20% 35V	Code no. 26486-219P

Page 27, para. 22

Change C27 to read Tant 4.7µF 20% 35V	Code no. 26486-219P
C33 " " Tant 4.7µF 20% 35V	Code no. 26486-219P
C39 " " Tant 4.7µF 20% 35V	Code no. 26486-219P
Add C56 Tant 22µF 20% 15V	Code no. 26486-230B

Page 30, para. 22

Change R111 to read Met film 1.5kΩ 2% ¼W	Code no. 24773-277U
Add R128 Met film 100Ω 2% ¼W	Code no. 24773-249J

Page 61, para. 38 Unit AS5 - FM control

Change C57 to read Elec 22µF -20+100% 25V	Code no. 26415-805K

Chap. 7 SERVICING DIAGRAMS

Page 31, Fig. 15 Divider chain (AA11)

Add electrolytic capacitor C59 value 220µF between the -5 V supply rail and earth, +ve connection to earth.

Page 33, Fig. 16 Amplitude modulator (AA21)

Change C8 to read 22µF
" C21 " " 4.7µF
" C39 " " 4.7µF
" R111 to read 1.5kΩ

Page 33, Fig. 16 Amplitude modulator (AA21) (contd.)

Add C56 electrolytic capacitor value 22µF connected in parallel with C38, +ve connection to the junction of L20/C38.
Add R128 value 100Ω between +12 V supply rail and the junction of L20/C38.

Chap. 7, Page 33, Fig. 16

Change the position of C27 and C33, shown terminating at TP9 and TP11, to connect instead to the collectors of TR26 and TR30.
Also change the value of both capacitors to 4.7µF.

Page 53, Fig. 26 Modulation leveller (AS3)

Change R10 to read 5kΩ
R58 " " 1kΩ

Page 57, Fig. 28 FM control (AS5)

Change C57 to read 22µF.

Page 49, Fig. 24 Latches, AS2, circuit diagram, sheet 1

Replace existing AS2, circuit diagram, sheet 1, by the Circuit Diagram 44828-343E included with this Manual Change for instruments with serial numbers prefixed 118201 or 118202.

Page 51, Fig. 25 Latches AS2, circuit diagram, sheet 2

Fig. 25 should be removed for instruments with serial numbers prefixed 118201 or 118202. The VCO steering, master oscillator supply and motor drive circuits illustrated on this diagram are situated on boards AS6, AS7A/AS7B and are shown on Figs. 32 and 33 instead.

EQUIPMENT	2017
TITLE	10 kHz-1024 MHz AM/FM SIGNAL GENERATOR
CODE NO.	52017-900K
SER.NOS.	118202 onwards
ACCOMPANYING DOCUMENTS	None

MANUAL CHANGE

As part of the policy of continuous development minor changes have been carried out to this equipment, amend the Service Manual as follows :-

Chap. 6 REPLACEABLE PARTS

Page 8, para. 12 Unit AP2 - Voltage stabilizers

Change the reference C1 to read C2 and insert on the line above

C1 Elec 4.7µF 5% 63V Code no. 26415-801M

Page 13, para. 16 Unit AL3 - Microprocessor system

Add the following information after IC11 :-

IC12 C8755A
IC13 C8755A
IC14 B2716
IC18 B2716

} Supplied as a set of 4 Code no. 44533-013G

Page 14, para. 16 contd.

Change IC21 ⚠ EPROM B1702AL2 Code no. 44533-013G
to read Code no. 28471-008E

Page 15, para. 17 Unit AL4 - Synchronizer/counter 'B'

Change IC21 74LS00 Code no. 28466-345H
to read IC21 74S00 Code no. 28466-331D

Page 23, para. 21 Unit AA11 - Divider chain

Add C60 Cer 15pF ±5% 63V Code no. 26343-467U

Page 55, para. 33 Unit AS1 - Master oscillator

Change D1 1N5145 Variable capacitor Code no. 28381-526K
to read D1 DVH 6760-25 Variable capacitor Code no. 44990-301K

Page 68, para. 45 Unit AR1A - RPP detector

Change	R4	Carb 10MΩ resistor to read R5	
Change	R17	Met film 22kΩ 2% ¼W	Code no. 24773-305R
to read	R17	Met film 4.7kΩ 2% ¼W	Code no. 24773-289W

Chap. 7 SERVICING DIAGRAMS

Page 23, Fig. 11 Synchronizer/counter 'B' (AL4)

Change IC21 74LS00 to read 74S00

Page 31, Fig. 15 Divider chain (AA11)

Add C60 15p capacitor connected in parallel with R14

Page 45, Fig. 22 Master oscillator (AS1)

Change D1 1N5145 to read DVH 6760-25

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Page 68, para. 45 Unit AR1A - RPP detector

Change	R4	Carb 10MΩ resistor to read R5	
Change	R17	Met film 22kΩ 2% ¼W	Code no. 24773-305R
to read	R17	Met film 4.7kΩ 2% ¼W	Code no. 24773-289W

Chap. 7 SERVICING DIAGRAMS

Page 23, Fig. 11 Synchronizer/counter 'B' (AL4)

Change IC21 74LS00 to read 74S00

Page 31, Fig. 15 Divider chain (AA11)

Add C60 15p capacitor connected in parallel with R14

Page 45, Fig. 22 Master oscillator (AS1)

Change D1 1N5145 to read DVH 6760-25

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MP MASTER
MA30771